

# AMD TR4(X399)

## Promontry 300-Series

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# MS-7B09 Ver:2.0

**CPU:**  
AMD TR4  
**System Chipset:**  
Promontory X399  
(X399 GAMING PRO CARBON AC)

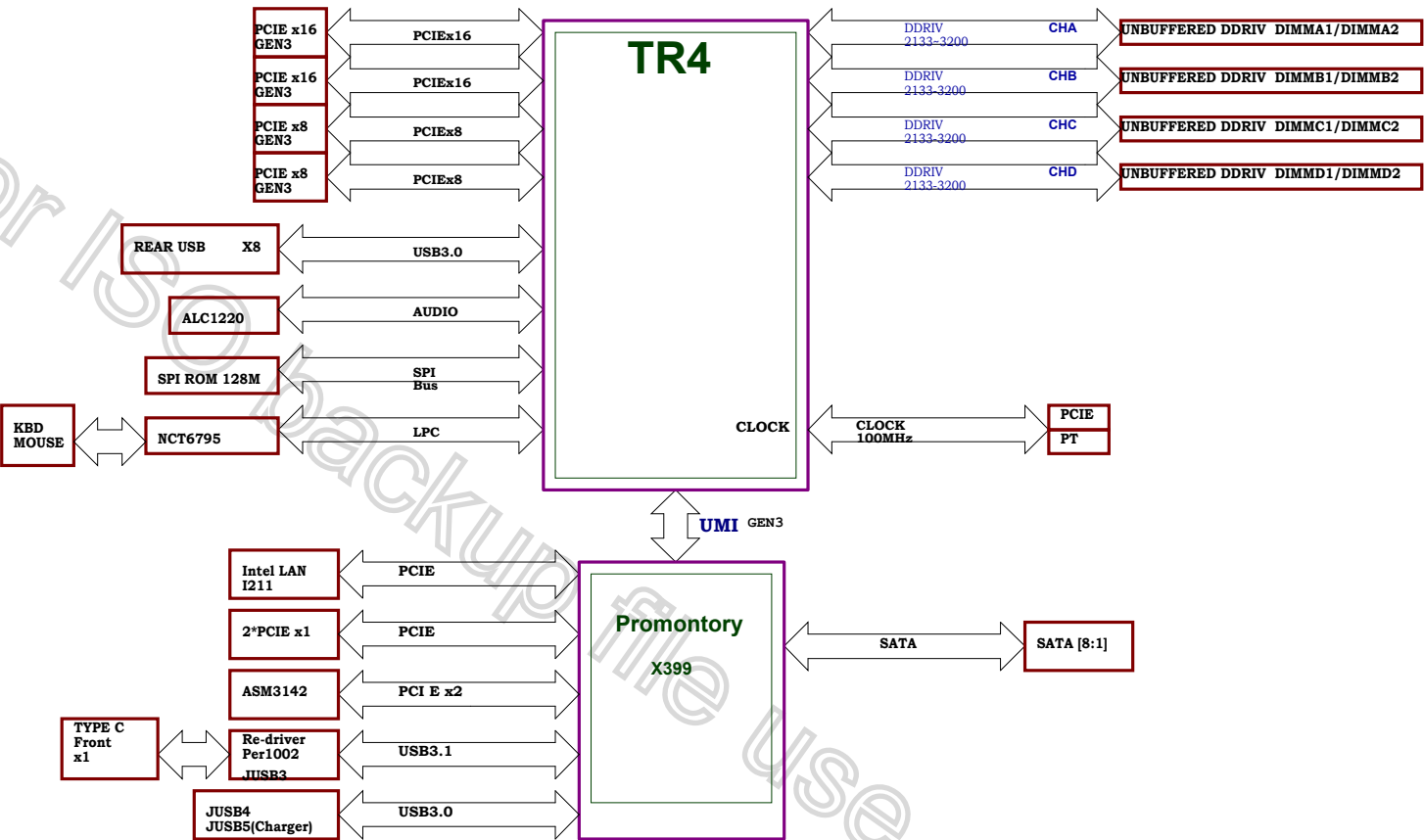
**Main Memory:**  
DDR IV \* 8 MAX:256 GB

**VRM**  
IR35201-10Phase  
IR35201-3Phase

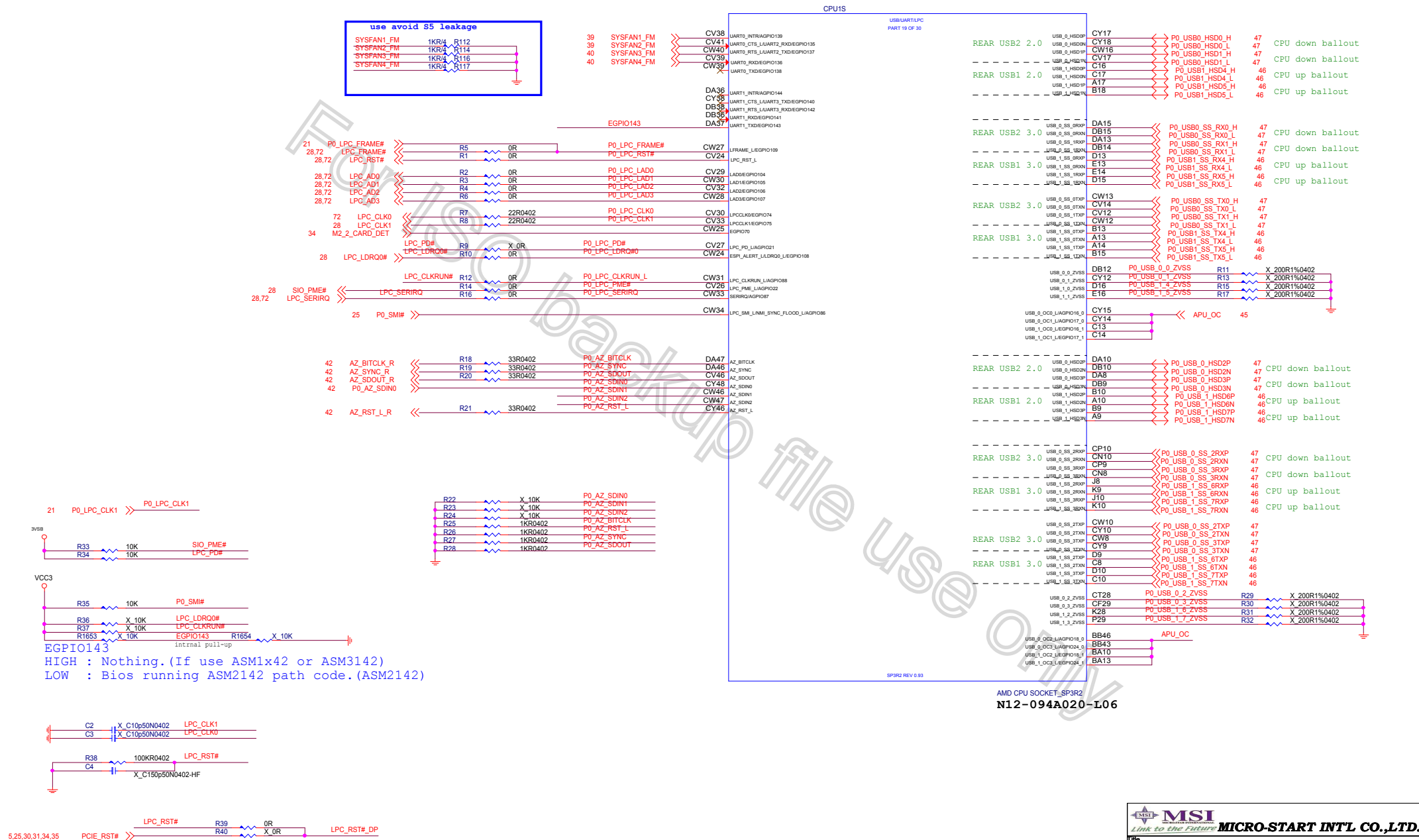
**On Board Chipset:**  
LPC Super I/O --NCT6975  
LAN Intel I211  
Azalia CODEC - Realtek ALC1220

**Expansion Slots:**  
From CPU  
PCI Express X16 Slot \* 2  
PCI Express X8 Slot \* 2  
From FCH  
PCI Express X1 Slot \* 2

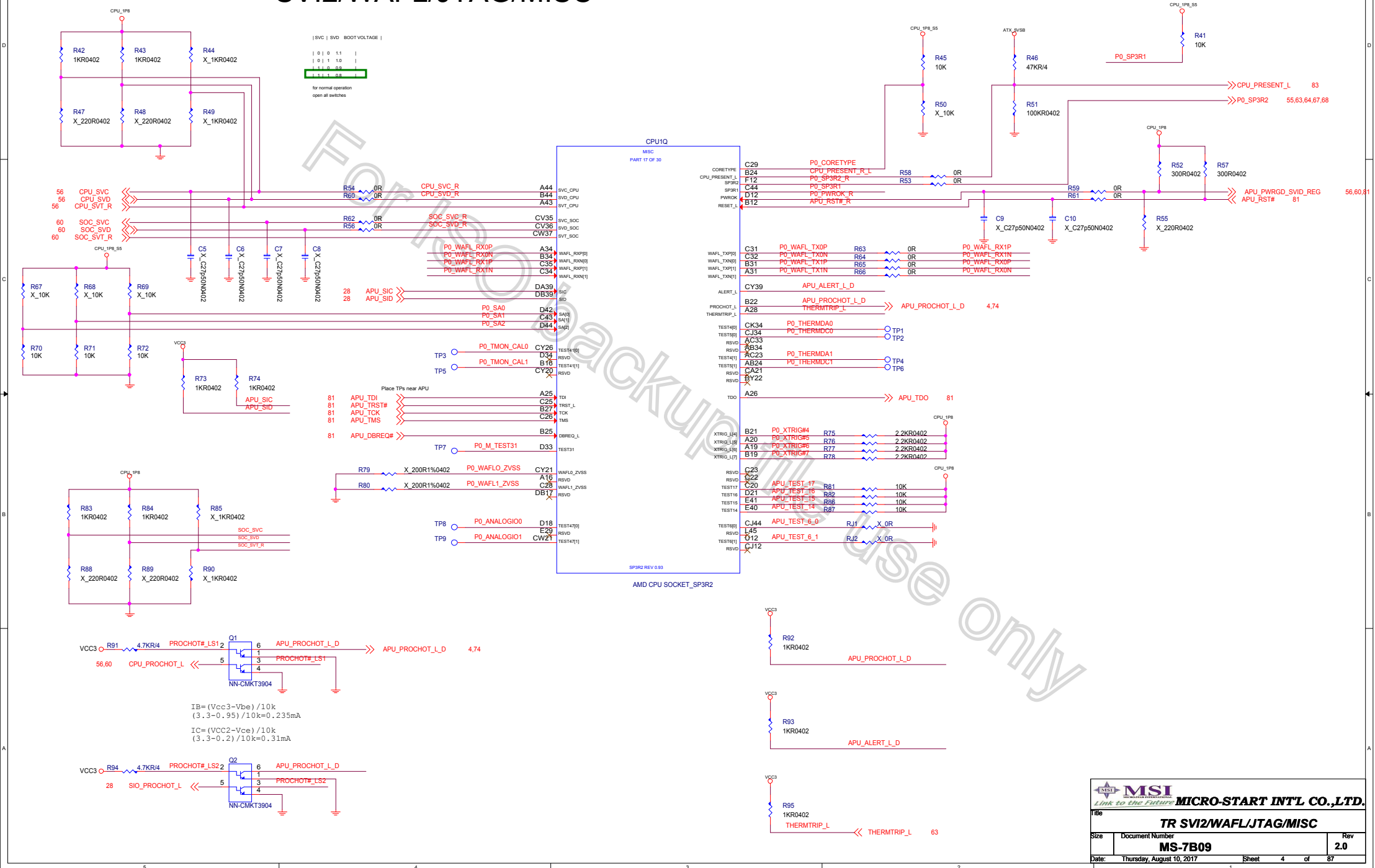
## X399 BLOCK DIAGRAM



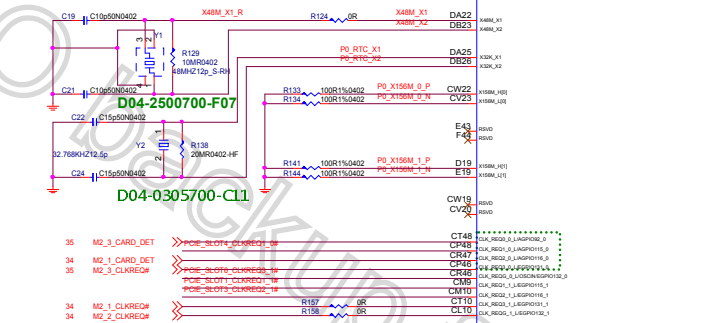
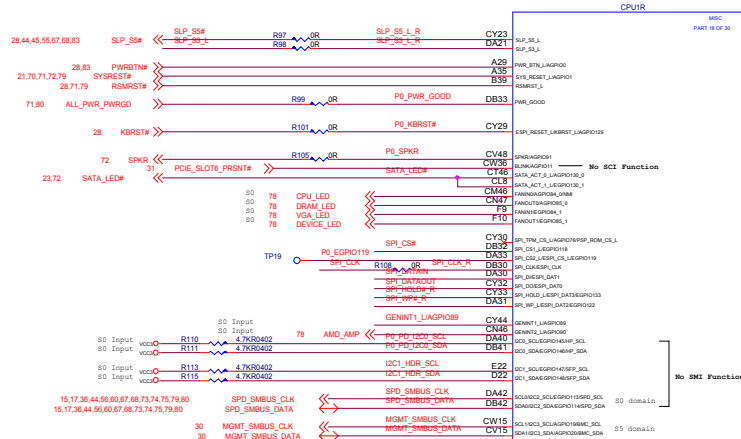
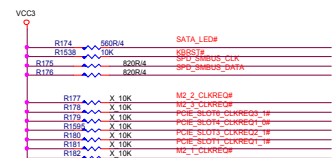
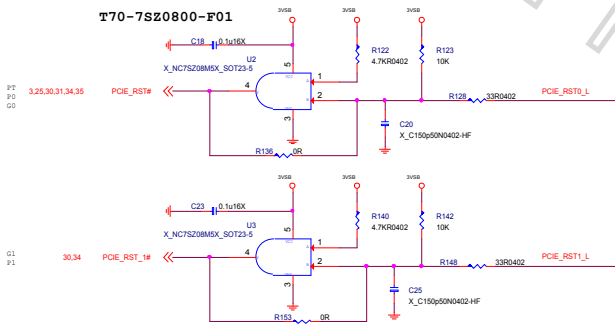
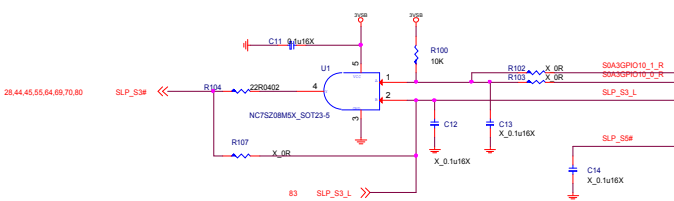
# USB/LPC/UART/HDA



## SVI2/WAFL/JTAG/MISC

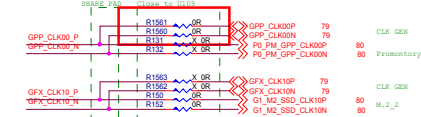
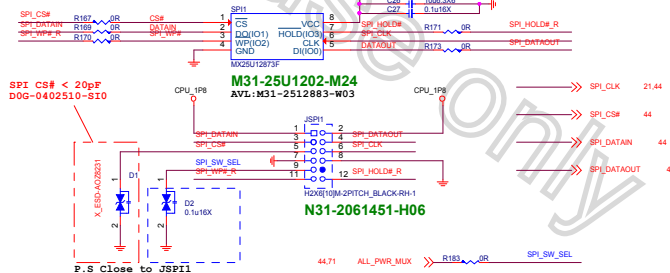
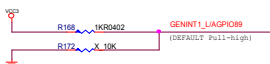


## ACPI/SPI/I2C/CLK/GPIO



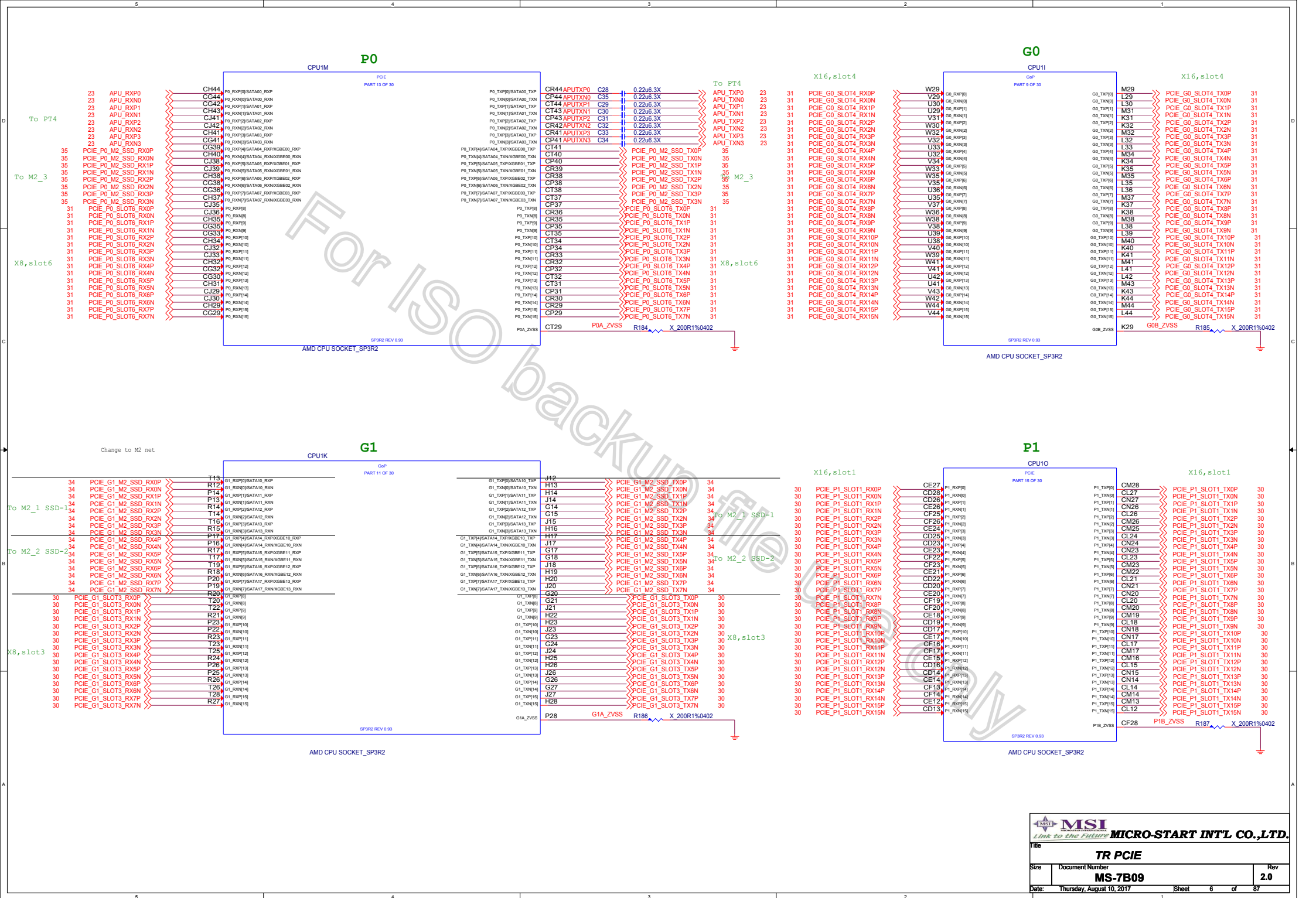
```
AMD DOCUMENT NUMBER: 105_D12700_00B
DATE: Mon Jan 23 14:21:00 2017
NOTE:
CLK REQ[3:0] 0 L ARE NOT SUPPORTED ON THREADRIPPER.
PIN CT48, CP48, CR47 AND CP46 CAN ONLY BE USED AS GPIO
```

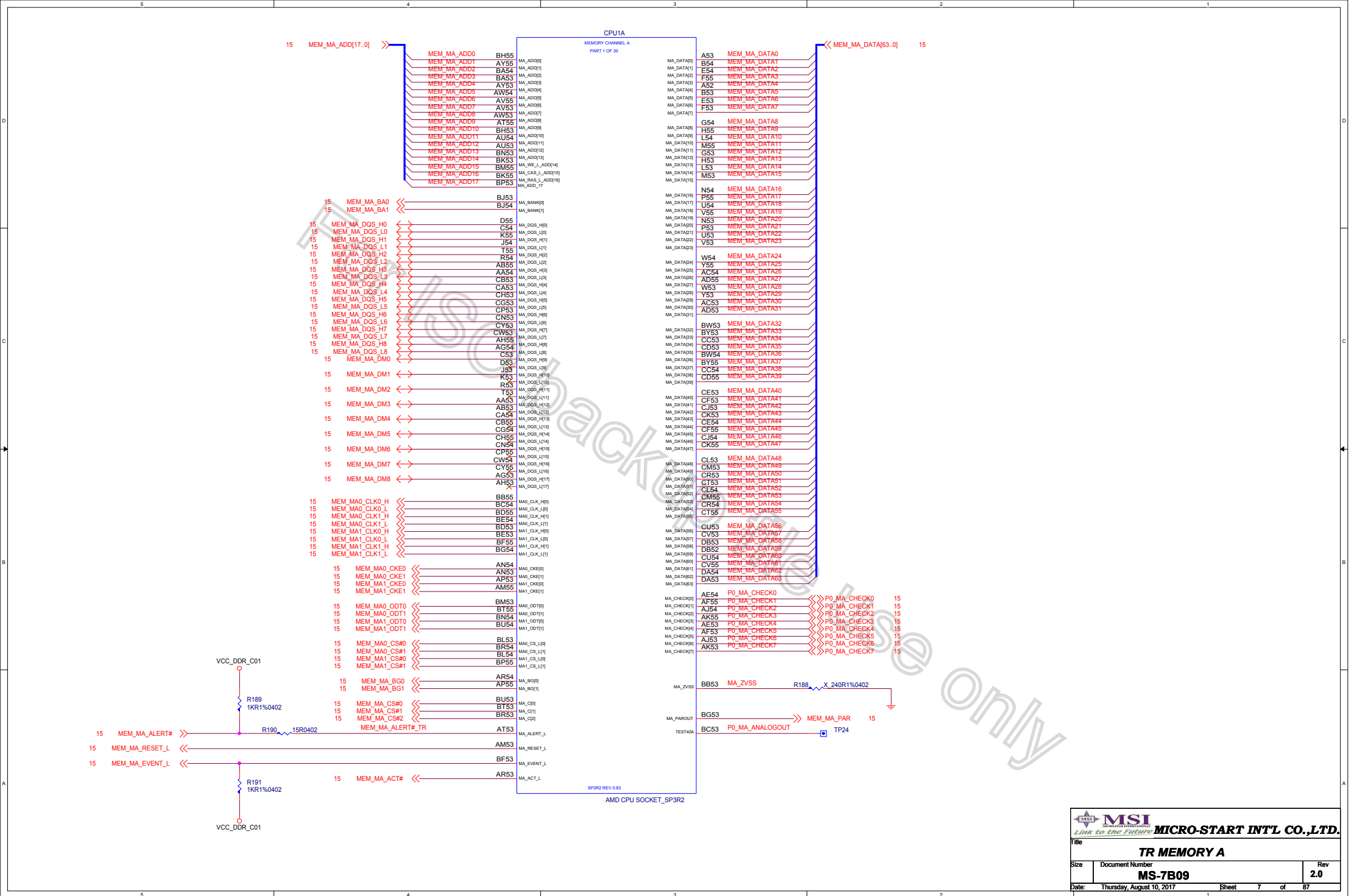
SPI ROM (1.8V)

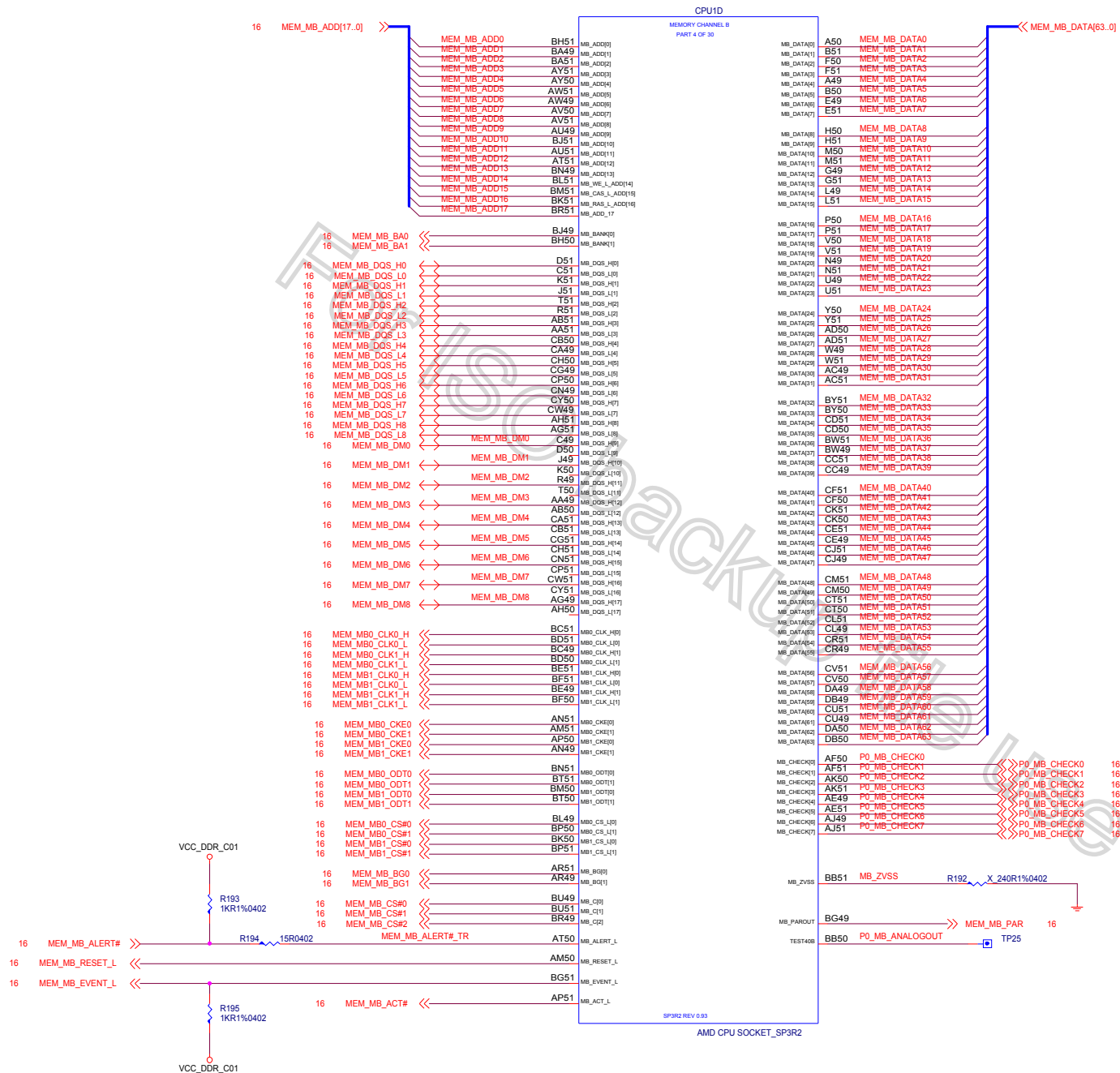


N12-094A020-L06

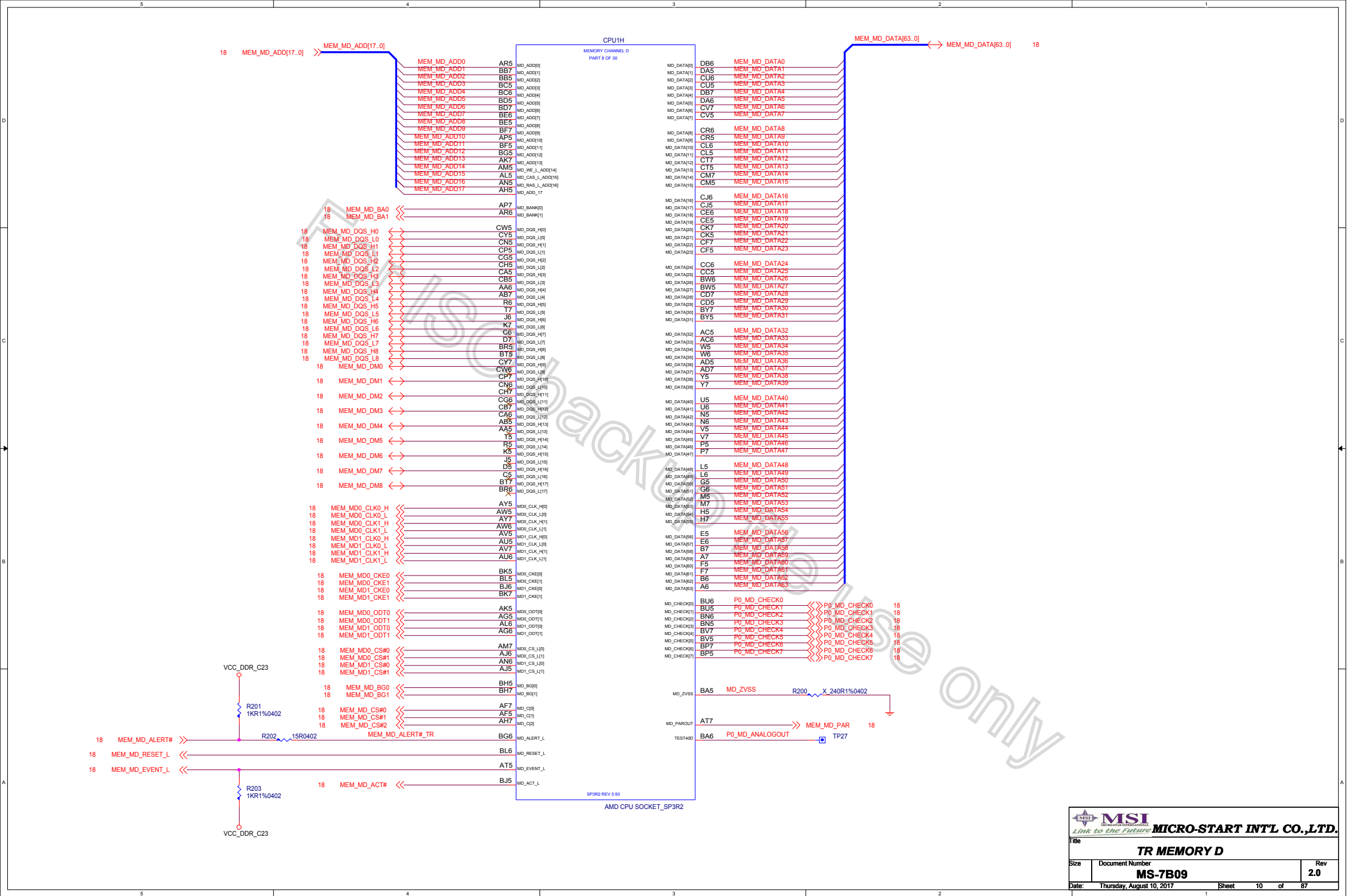




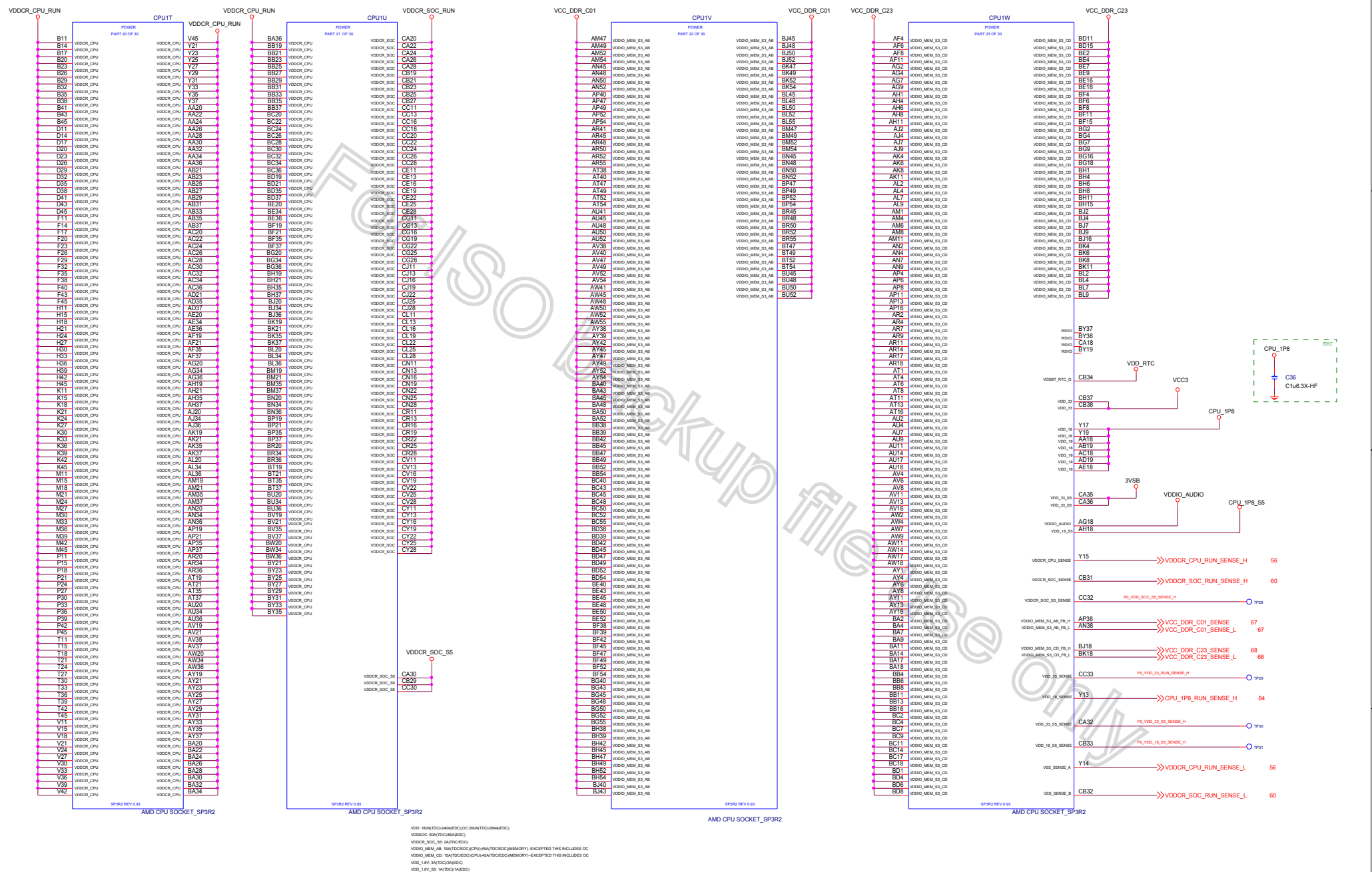


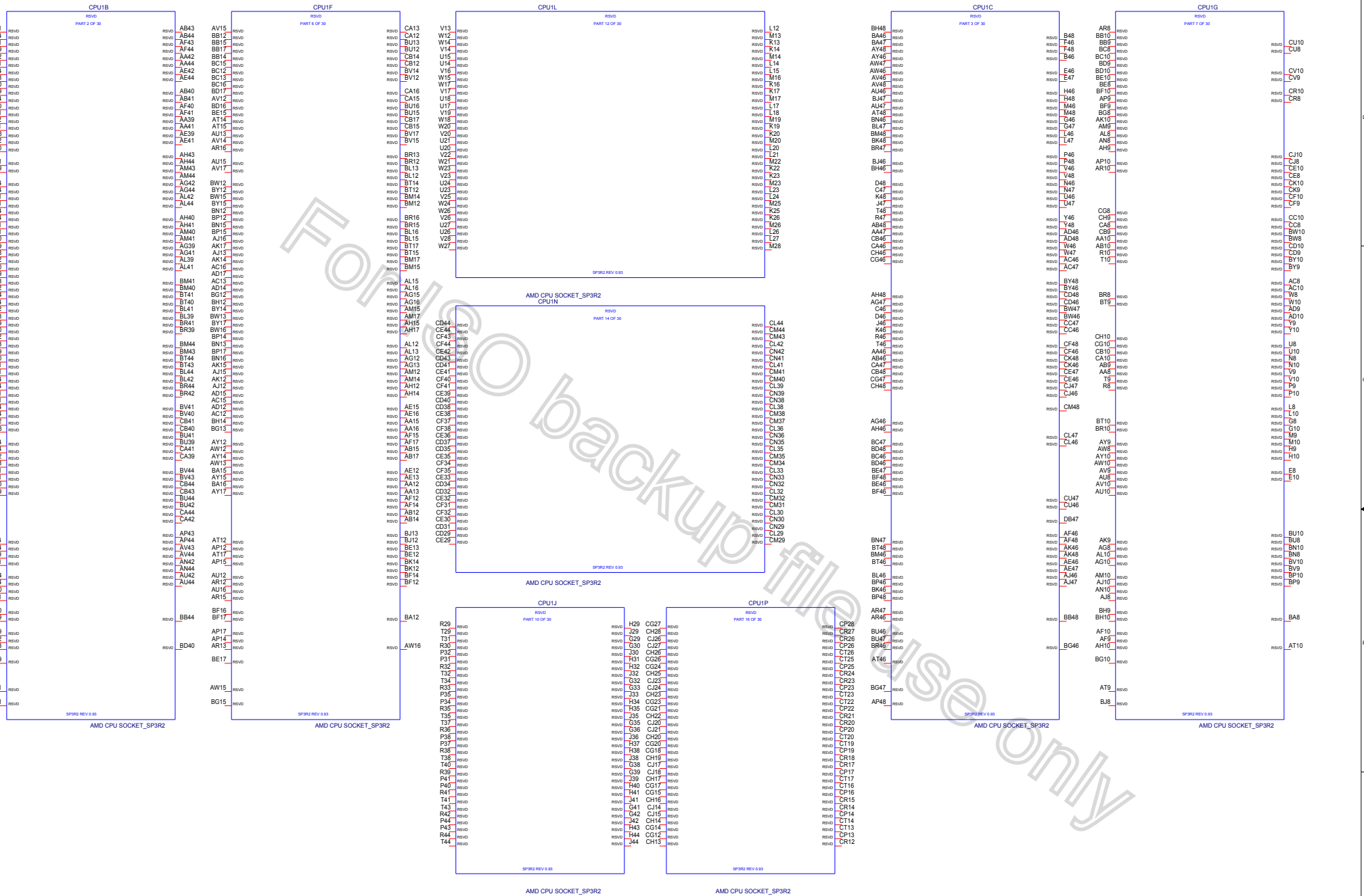






# POWER



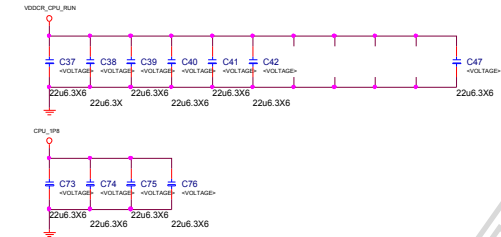


17ci203

VDDCR\_CPU Bottom Side Decoupling:

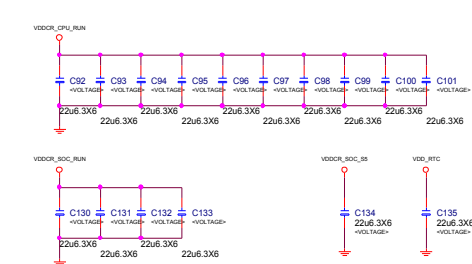
Bottom Side - Mirrored with Top Cavity - North

OEM Skt: 15; SLT Skt: 13



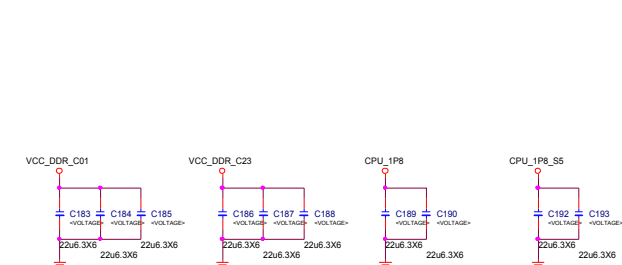
Bottom Side - Mirrored with Top Cavity - South

OEM Skt: 15; SLT Skt: 13



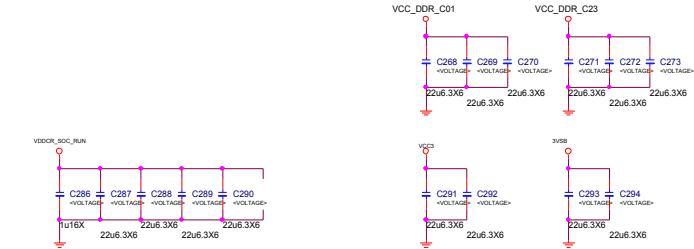
Bottom Side - North

OEM Skt: 24; SLT Skt: 24



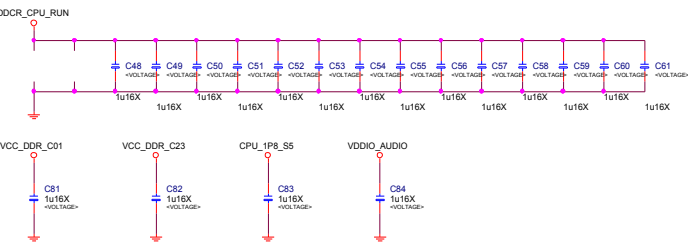
Bottom Side - South

OEM Skt: 24; SLT Skt: 24



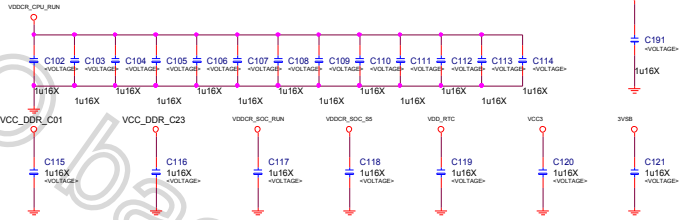
Bottom Side - North

OEM Skt: 20; SLT Skt: 20



Bottom Side - South

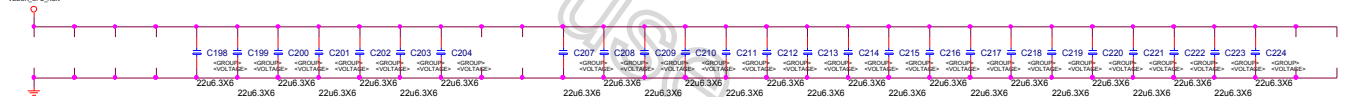
EM Skt: 20; SLT Skt: 20



Bottom Side - In the socket split regions

OEM SKT ONLY; NOT AVAILABLE IN SLT; CAN BE USED FOR RESISTORS

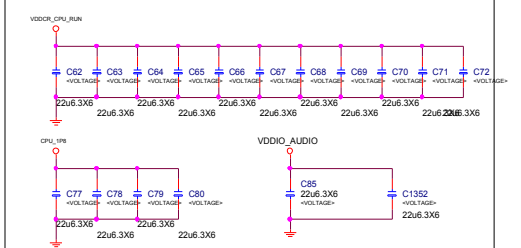
## RSVD FOR OVER CLOCKING



Top Side Decoupling:

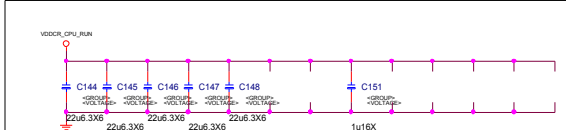
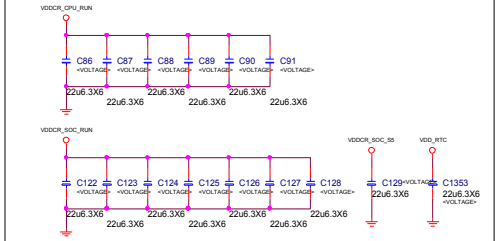
Top Cavity - North Decoupling

OEM Skt: 15; SLT Skt: 13

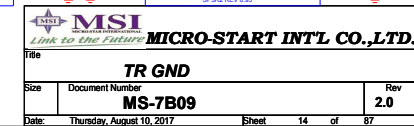


Top Cavity South Decoupling

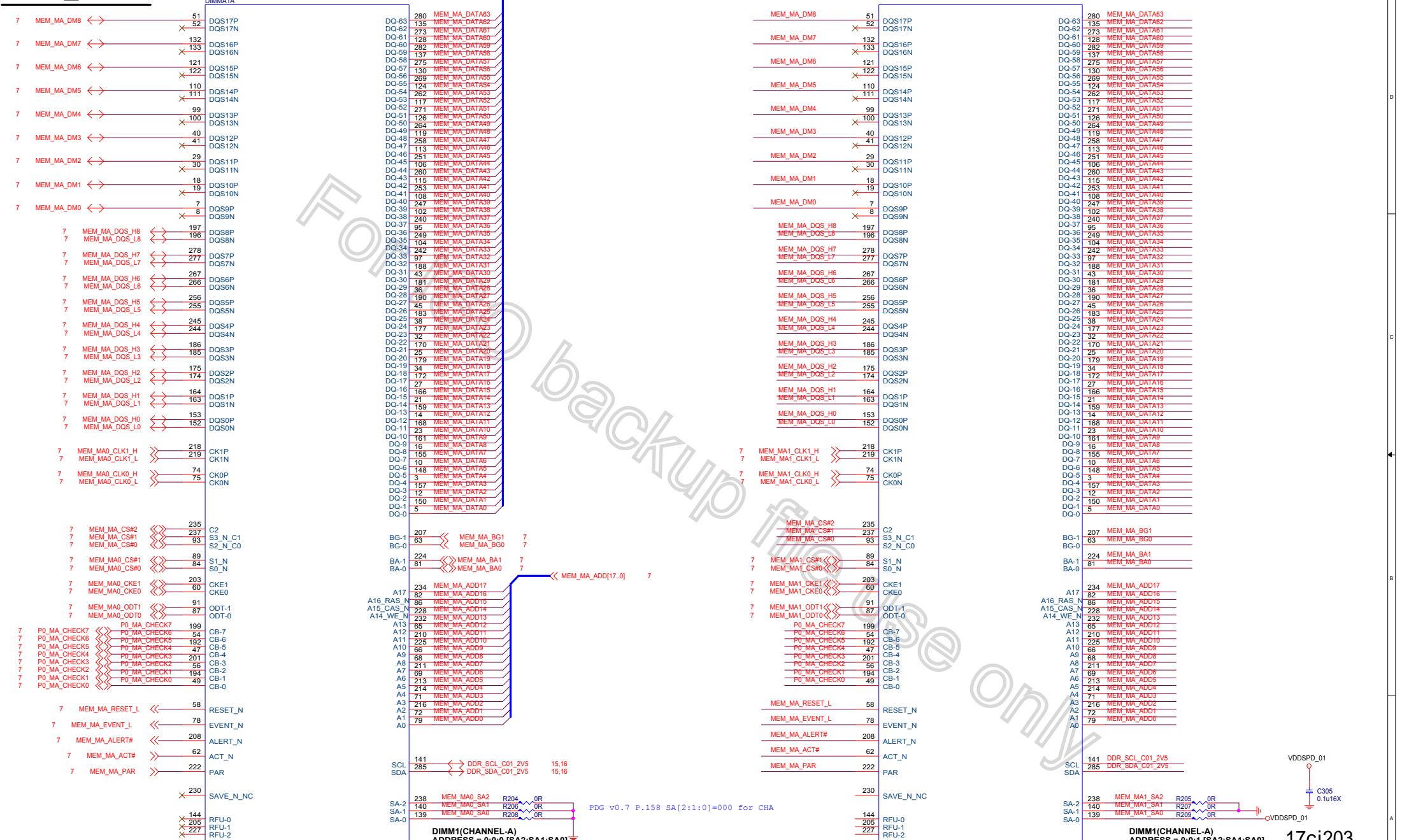
OEM Skt: 15; SLT Skt: 13



17ci203



DIMM\_A1/A2

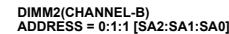


DIMMB1A



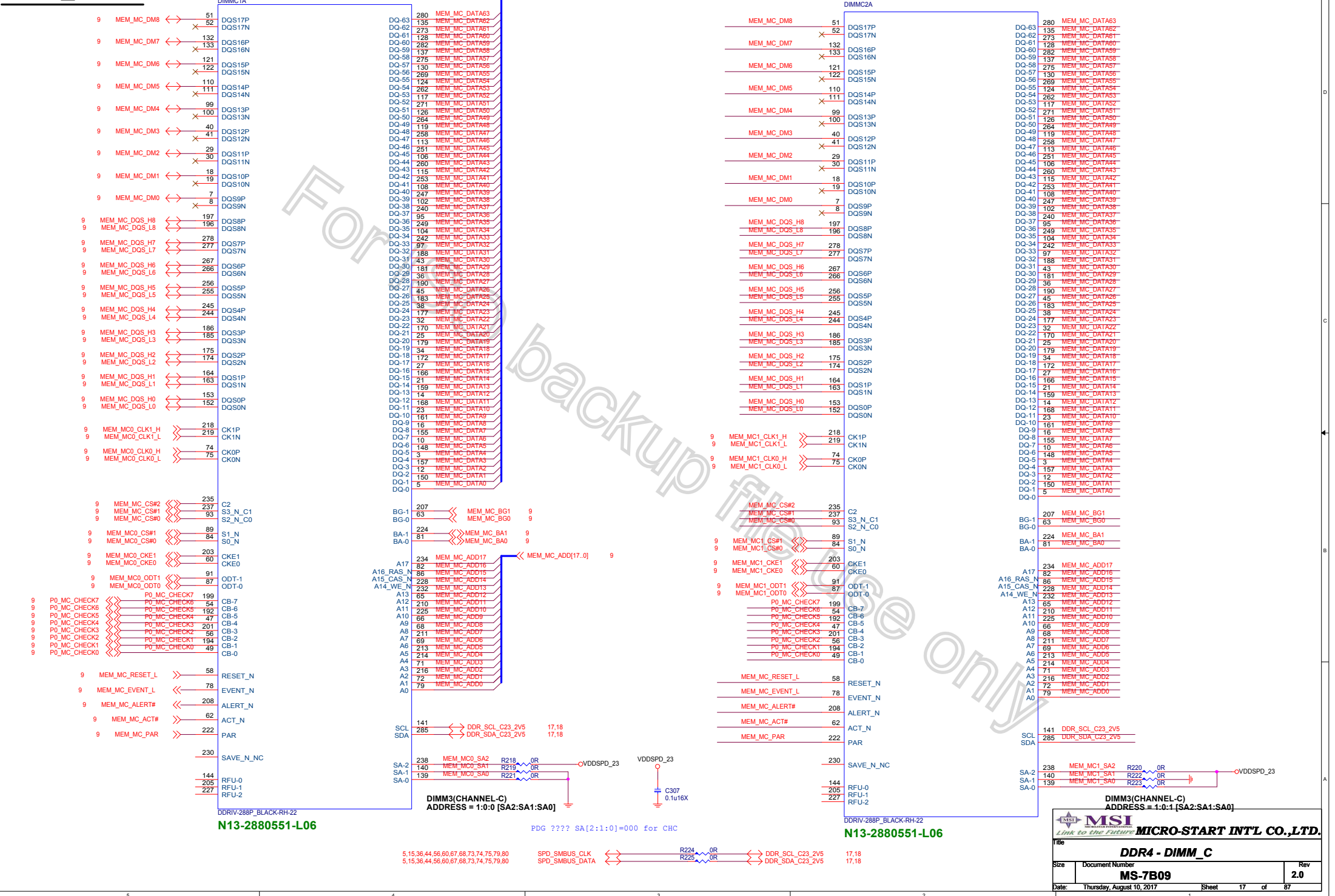
**DIMM2(CHANNEL-B)**  
**ADDRESS = 0:1:0 [SA2:SA1:SA0]**

PDG v0.7 P.158 SA[2:1:0]=010 for CHB



Title			
<b>DDR4 - DIMM_B</b>			
Size	Document Number	Rev	
	<b>MS-7B09</b>	<b>2.0</b>	
Date:	Thursday, August 10, 2017	Sheet	16 of 87

DIMM\_C1/C2



**MSI**  
Link to the future

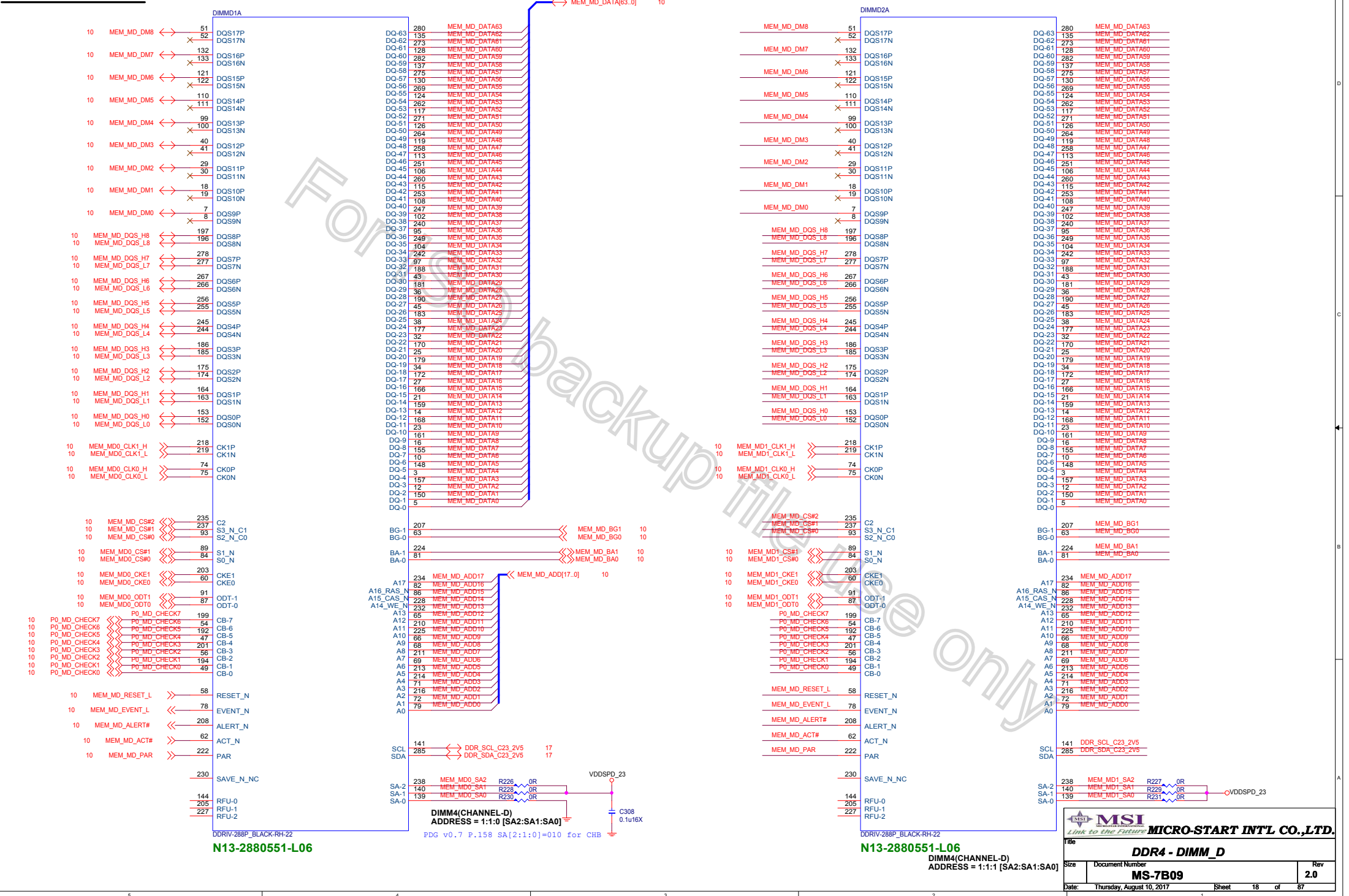
**MICRO-START INTL CO.,LTD.**

File: **DDR4 - DIMM\_C**

Size: Document Number: Rev: **2.0**

Date: Thursday, August 10, 2017 Sheet: 17 of 87

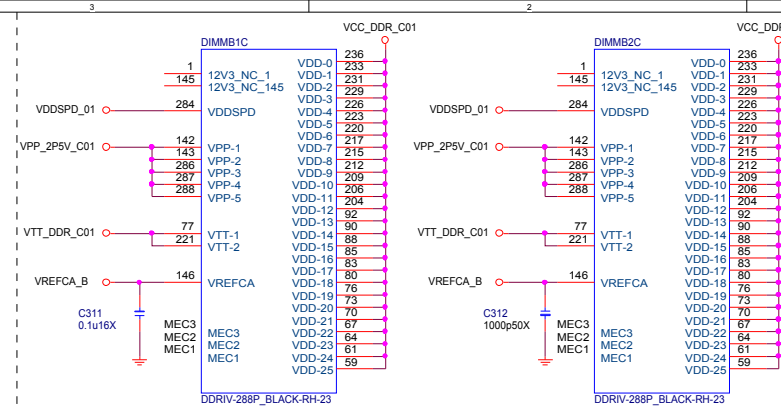
DIMM\_D1/D2



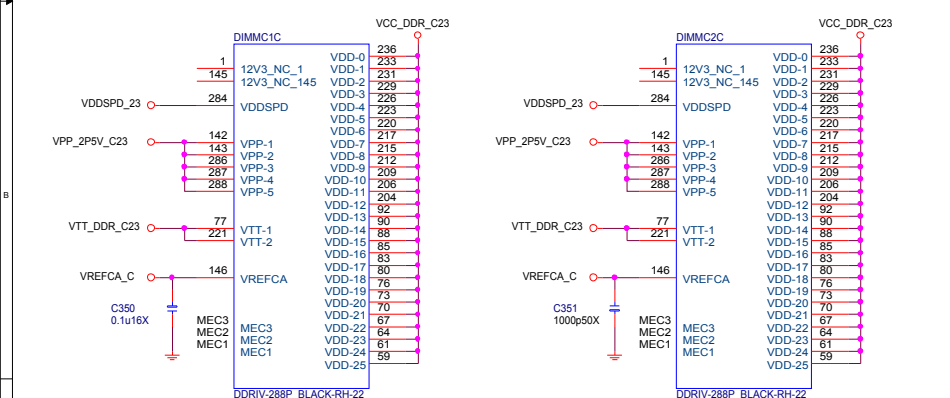
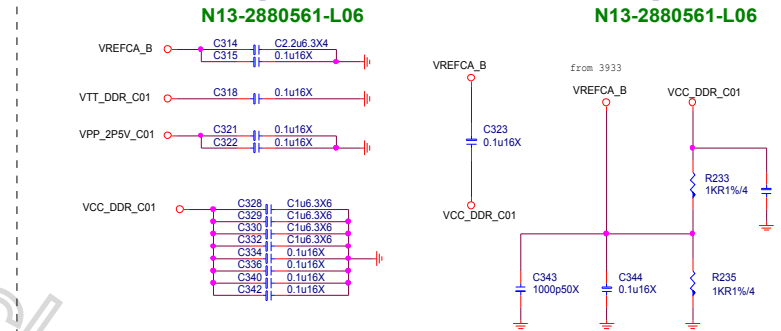
N13-2880551-L06

N13-2880551-L06

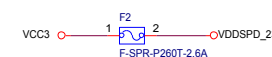
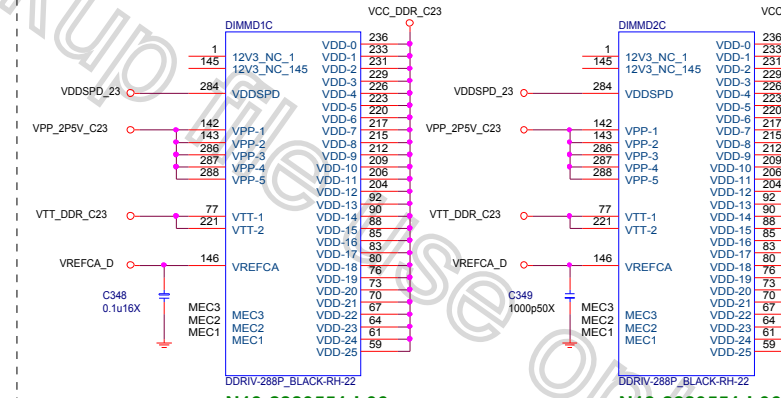
MSI Link to the future			MICRO-START INTL CO.,LTD.					
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DDR4 - DIMM_D								
Size	Document Number				Rev			
	MS-7B09				2.0			
Date:	Thursday, August 10, 2017	Sheet	18	of	87			

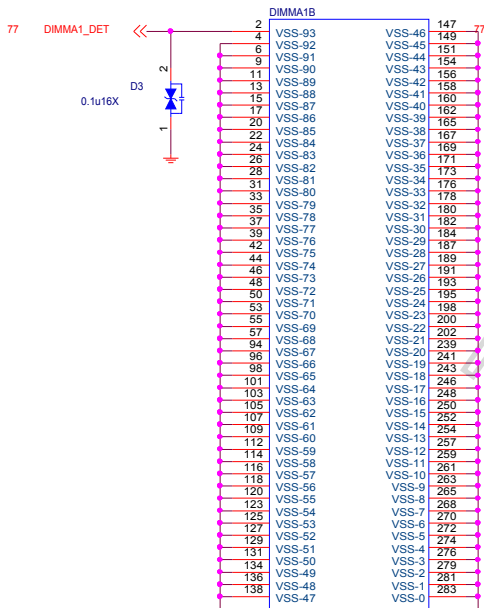


(place resistors close to DIMMs)

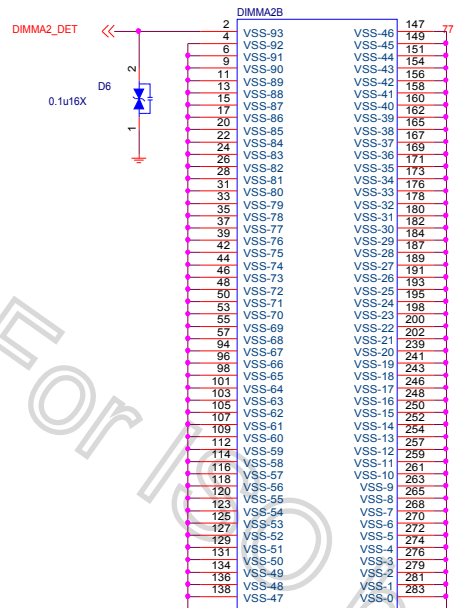


(place resistors close to DIMMs)

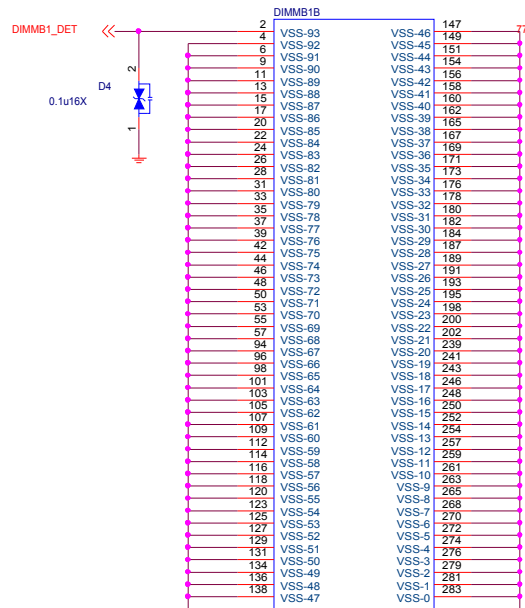




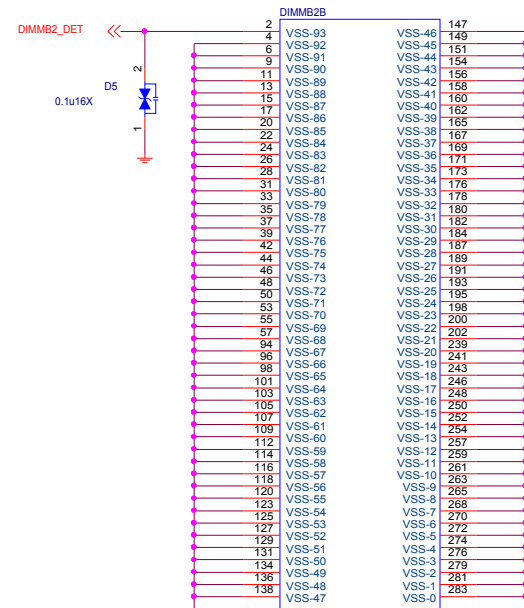
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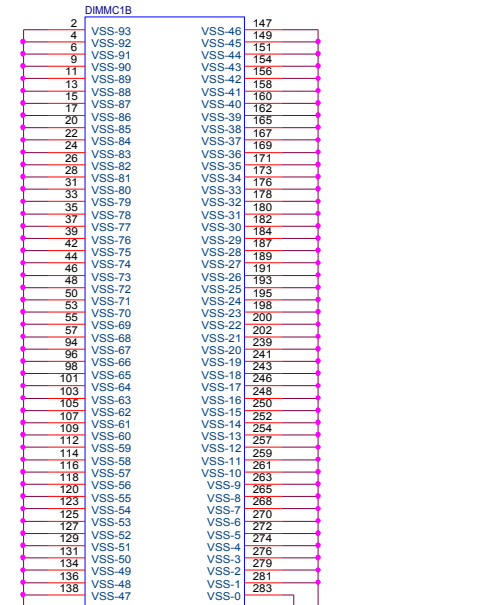
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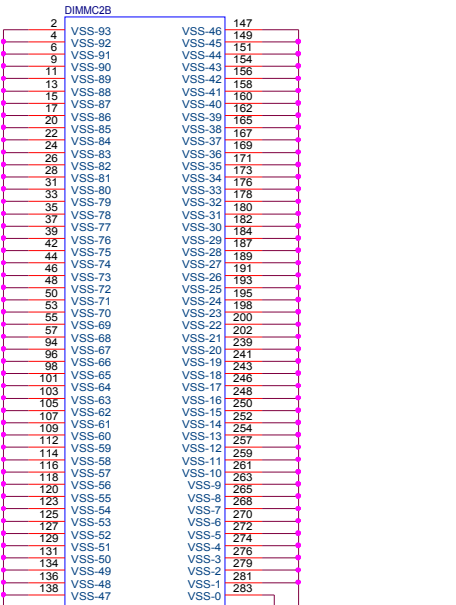
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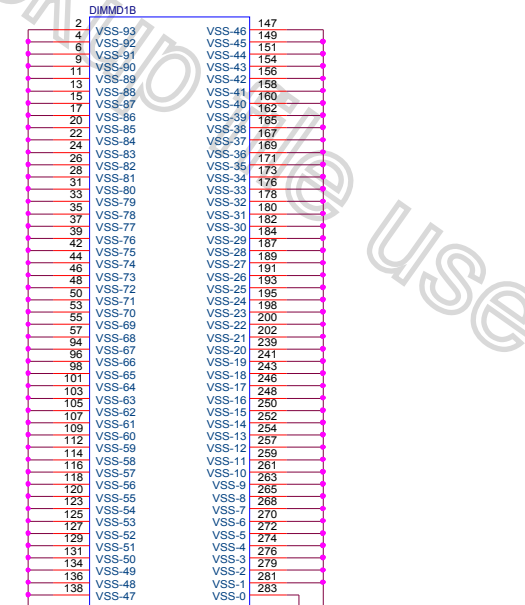
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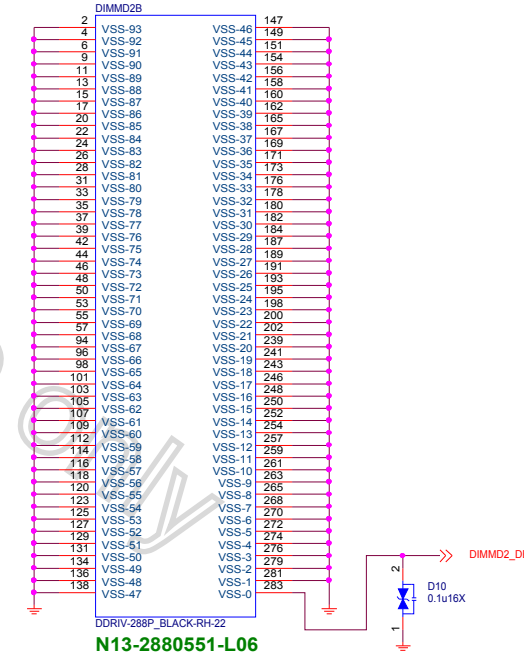
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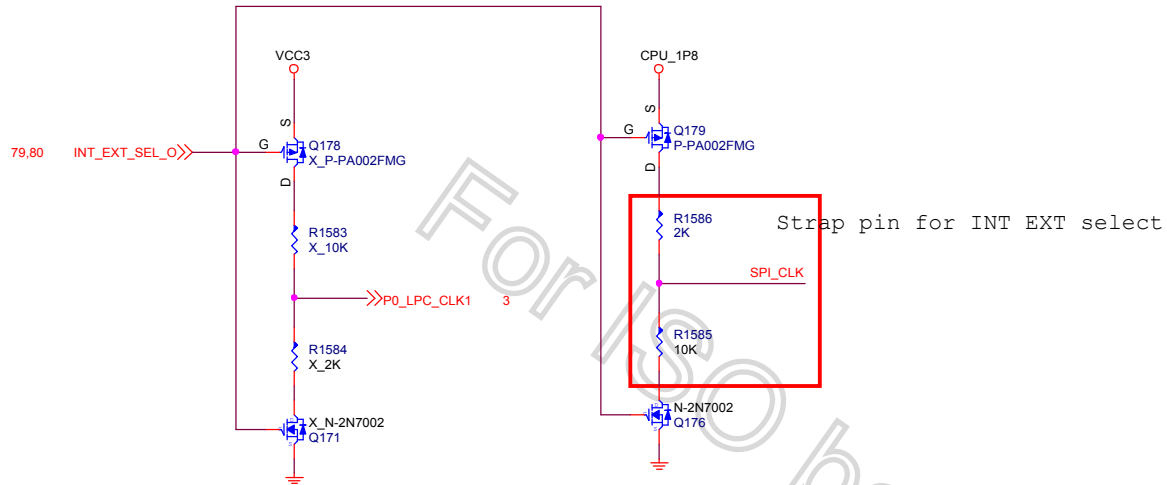
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N13-2880551-L06

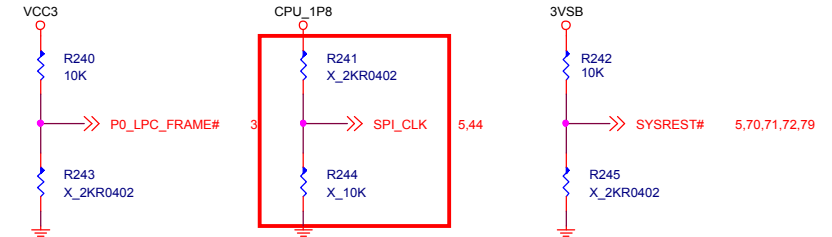


N13-2880551-L06



## CPU STRAPS

STRAP	DEFINITION
SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE
LPC_FRAME_L	ROM TYPE SELECT 1:BOOT FROM SPI ROM(DEFAULT) 0:BOOT FROM LPC ROM

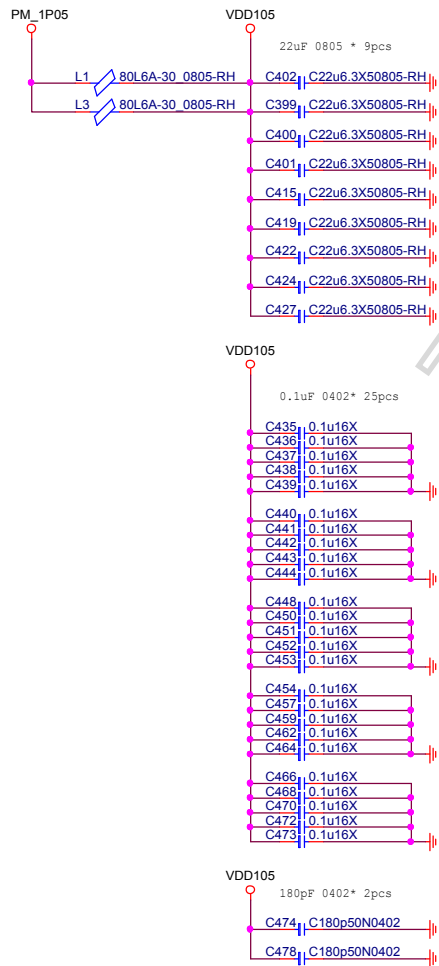












5.5A

VDD105

H15 VDD105\_0

H17 VDD105\_1

J11 VDD105\_2

K8 VDD105\_3

K9 VDD105\_4

K13 VDD105\_5

K14 VDD105\_6

K17 VDD105\_7

L8 VDD105\_8

L17 VDD105\_9

M17 VDD105\_10

N17 VDD105\_11

P7 VDD105\_12

P8 VDD105\_13

P17 VDD105\_14

R1 VDD105\_15

R2 VDD105\_16

R3 VDD105\_17

R4 VDD105\_18

R5 VDD105\_19

R6 VDD105\_20

R7 VDD105\_21

R8 VDD105\_22

R17 VDD105\_23

T1 VDD105\_24

T2 VDD105\_25

T3 VDD105\_26

T4 VDD105\_27

T5 VDD105\_28

T6 VDD105\_29

T7 VDD105\_30

T8 VDD105\_31

T17 VDD105\_32

U1 VDD105\_33

U2 VDD105\_34

U3 VDD105\_35

U4 VDD105\_36

U5 VDD105\_37

U6 VDD105\_38

U7 VDD105\_39

U8 VDD105\_40

U17 VDD105\_41

V9 VDD105\_42

V10 VDD105\_43

V11 VDD105\_44

V14 VDD105\_45

V15 VDD105\_46

V16 VDD105\_47

V20 VDD105\_48

V21 VDD105\_49

W11 VDD105\_50

W13 VDD105\_51

W16 VDD105\_52

FCH1E

POWER

VCC25\_0 C1

VCC25\_1 C2

VCC25\_2 C3

VCC25\_3 D1

VCC25\_4 D2

VCC25\_5 D3

VCC25\_6 D4

VCC25\_7 D5

VCC25\_8 D6

VCC25\_9 E1

VCC25\_10 E2

VCC25\_11 E3

VCC25\_12 E4

VCC25\_13 E5

VCC25\_14 E6

VCC25\_15 F6

VCC25\_16 K11

VCC25\_17 K12

VCC25\_18 K15

VCC25\_19 K16

VCC25\_20 M8

VCC25\_21 M19

VCC25\_22 N8

VCC25\_23 N19

VCC25\_24 P19

VCC25\_25 R19

VCC25\_26 V13

VCC25\_27 V17

VCC25\_28

900mA

VCC25

G9 VCC33

L18 VCC33

Y20 VCC33\_2

V8 VSUS33

AA8 VSUS33\_1

AB8 VSUS33\_2

AC8 VSUS33\_3

AD8 VSUS33\_4

AE8 VSUS33\_5

AF8 VSUS33\_6

V7 VSUS105

W15 VSUS105\_1

200mA

70mA

50mA

PROMONTORY

AMD-218-0891007-00-RH

PM\_2P5V

VCC25

L2 80L6A-30 0805-RH

C403 C22u6.3X50805-RH

C407 C22u6.3X50805-RH

C411 C22u6.3X50805-RH

C413 C22u6.3X50805-RH

C417 C22u6.3X50805-RH

VCC3

VCC33

L4 80L6A-30 0805-RH

C445 C22u6.3X50805-RH

3VSB

VSUS33

L5 80L6A-30 0805-RH

C455 C22u6.3X50805-RH

C460 C22u6.3X50805-RH

PM\_1P05\_S5

VSUS105

L6 80L6A-30 0805-RH

C475 C22u6.3X50805-RH

C476 C22u6.3X50805-RH

C477 C22u6.3X50805-RH

C478 C22u6.3X50805-RH

C479 C22u6.3X50805-RH

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C503 C22u6.3X50805-RH

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C515 C22u6.3X50805-RH

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C519 C22u6.3X50805-RH

C520 C22u6.3X50805-RH

C521 C22u6.3X50805-RH

C522 C22u6.3X50805-RH

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C524 C22u6.3X50805-RH

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C526 C22u6.3X50805-RH

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C529 C22u6.3X50805-RH

C530 C22u6.3X50805-RH

C531 C22u6.3X50805-RH

C532 C22u6.3X50805-RH

C533 C22u6.3X50805-RH

C534 C22u6.3X50805-RH

C535 C22u6.3X50805-RH

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C537 C22u6.3X50805-RH

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C539 C22u6.3X50805-RH

C540 C22u6.3X50805-RH

C541 C22u6.3X50805-RH

C542 C22u6.3X50805-RH

C543 C22u6.3X50805-RH

C544 C22u6.3X50805-RH

C545 C22u6.3X50805-RH

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C548 C22u6.3X50805-RH

C549 C22u6.3X50805-RH

C550 C22u6.3X50805-RH

C551 C22u6.3X50805-RH

C552 C22u6.3X50805-RH

C553 C22u6.3X50805-RH

C554 C22u6.3X50805-RH

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C558 C22u6.3X50805-RH

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C561 C22u6.3X50805-RH

C562 C22u6.3X50805-RH

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C565 C22u6.3X50805-RH

C566 C22u6.3X50805-RH

C567 C22u6.3X50805-RH

C568 C22u6.3X50805-RH

C569 C22u6.3X50805-RH

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C574 C22u6.3X50805-RH

C575 C22u6.3X50805-RH

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C617 C22u6.3X50805-RH

C618 C22u6.3X50805-RH

C619 C22u6.3X50805-RH

C620 C22u6.3X50805-RH

C621 C22u6.3X50805-RH

C622 C22u6.3X50805-RH

C623 C22u6.3X50805-RH

C624 C22u6.3X50805-RH

C625 C22u6.3X50805-RH

C626 C22u6.3X50805-RH

C627 C22u6.3X50805-RH

C628 C22u6.3X50805-RH

C629 C22u6.3X50805-RH

C630 C22u6.3X50805-RH

C631 C22u6.3X50805-RH

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C640 C22u6.3X50805-RH

C641 C22u6.3X50805-RH

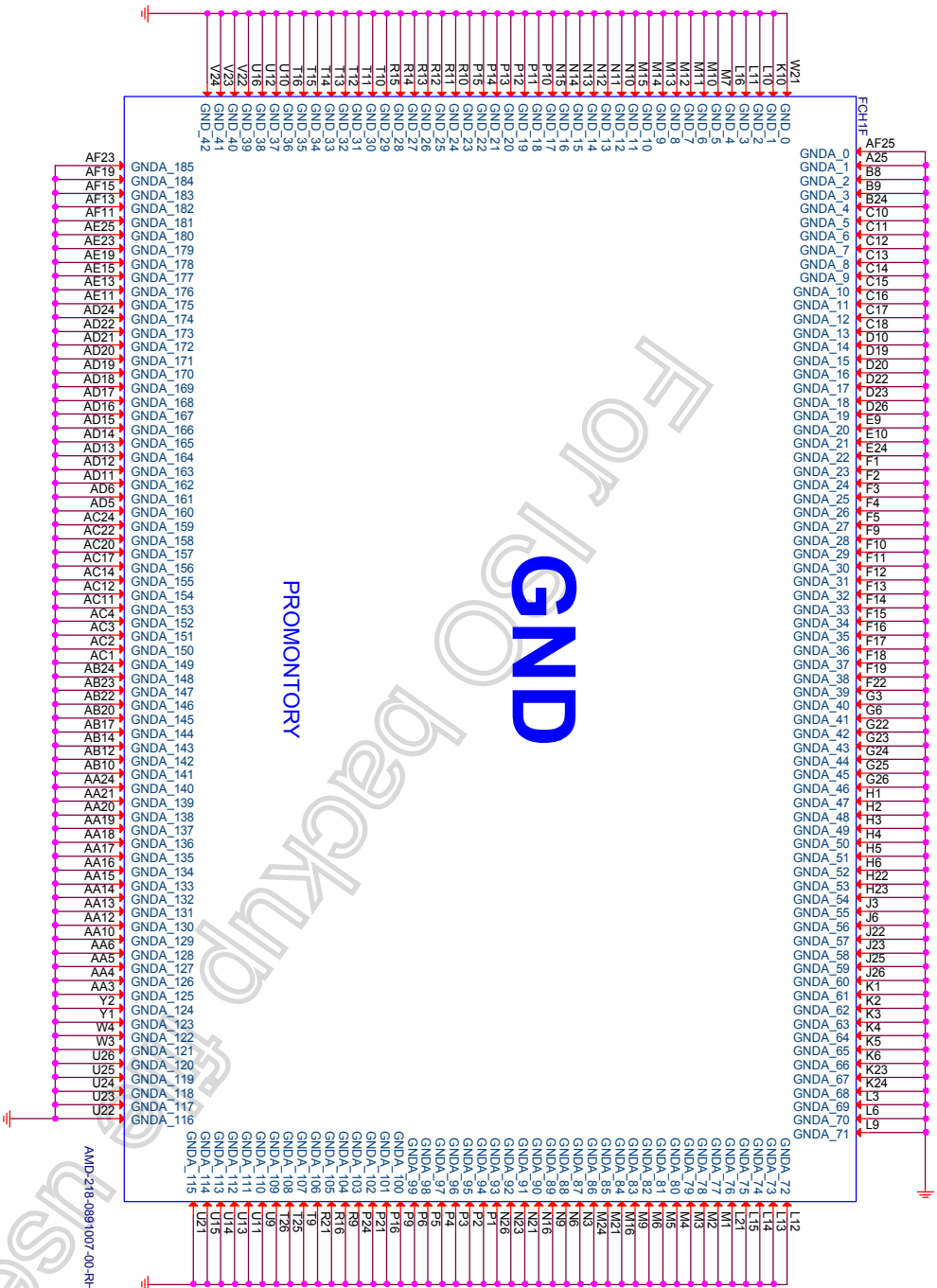
C642 C22u6.3X50805-RH

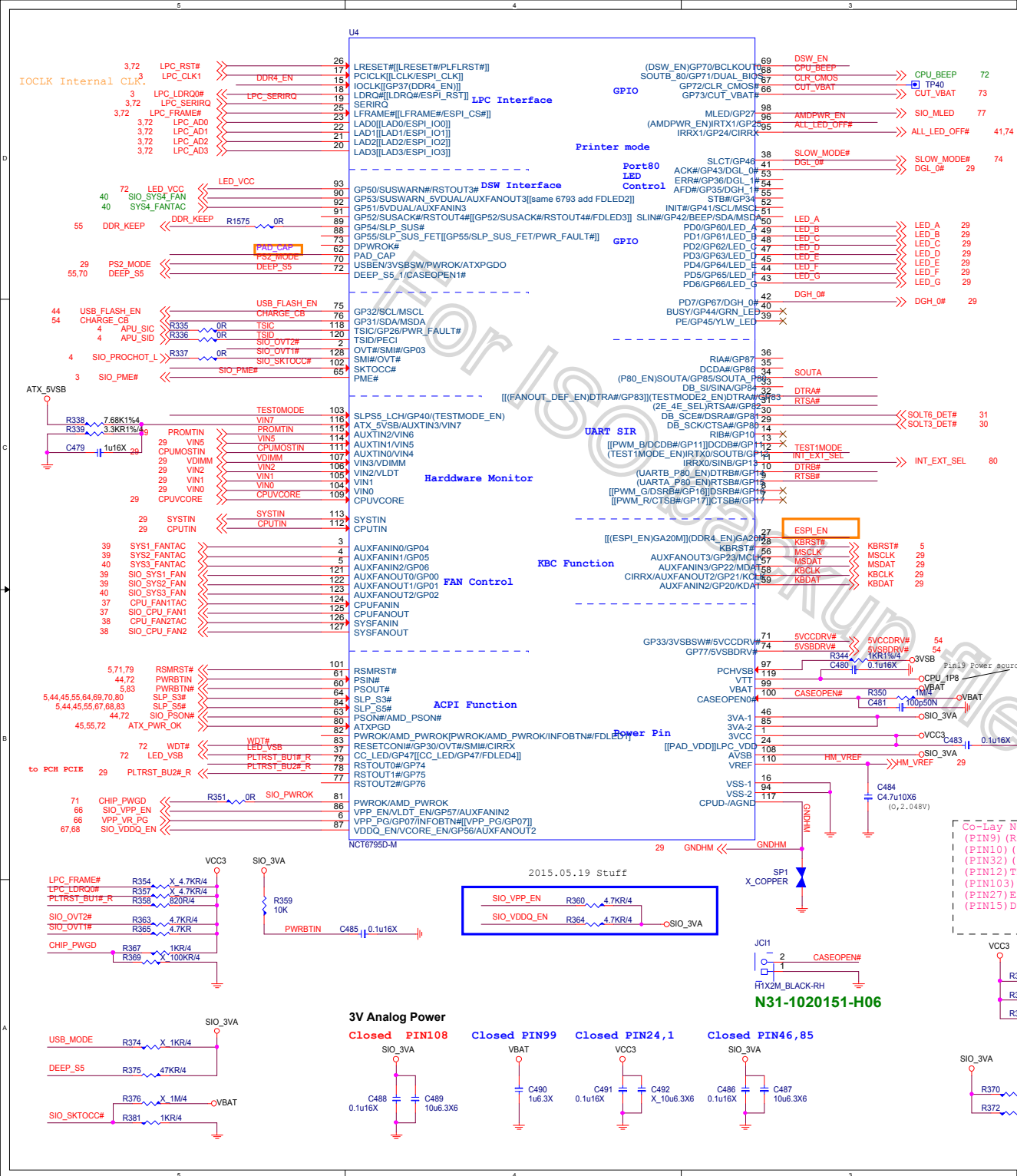
C643 C22u6.3X50805-RH

C644 C22u6.3X50805-RH

C645 C22u6.3X50805-RH

C64





POWER ON STRAPPING PIN FOR NCT6793/6795

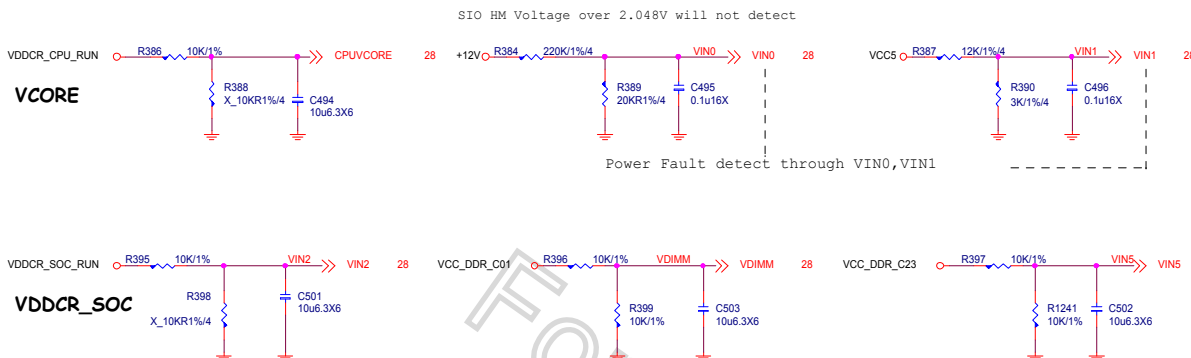
PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:  
If PIN34 strapping low, BIOS must programming LPT or GPIO

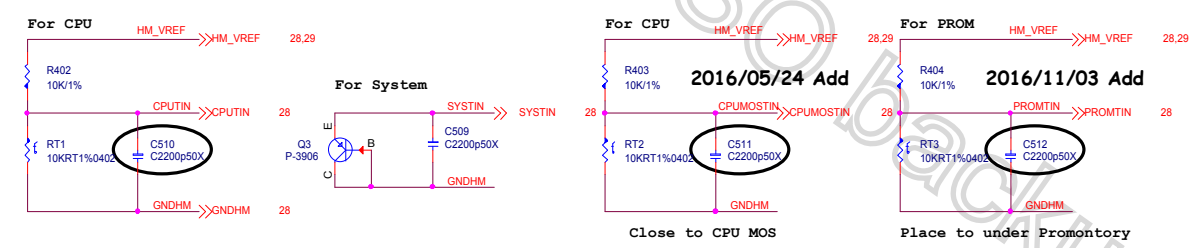
Co-Lay NCT6795  
(PIN9) (RTSB#) 80 ENA 0=Disable 1=Enable  
(PIN10) (DTRB#) 80 ENB 0=Disable 1=Enable  
(PIN32) (DTRA#) FANOUT 0=50% 1=100%  
(PIN12) TEST MODE EN1 0=Disable 1=Enable  
(PIN103) TEST MODE EN0 0=Disable 1=Enable  
(PIN27) ESPI EN0 0=LPC 1=ESPI  
(PIN15) DDR4\_EN 0=Disable 1=Enable

Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

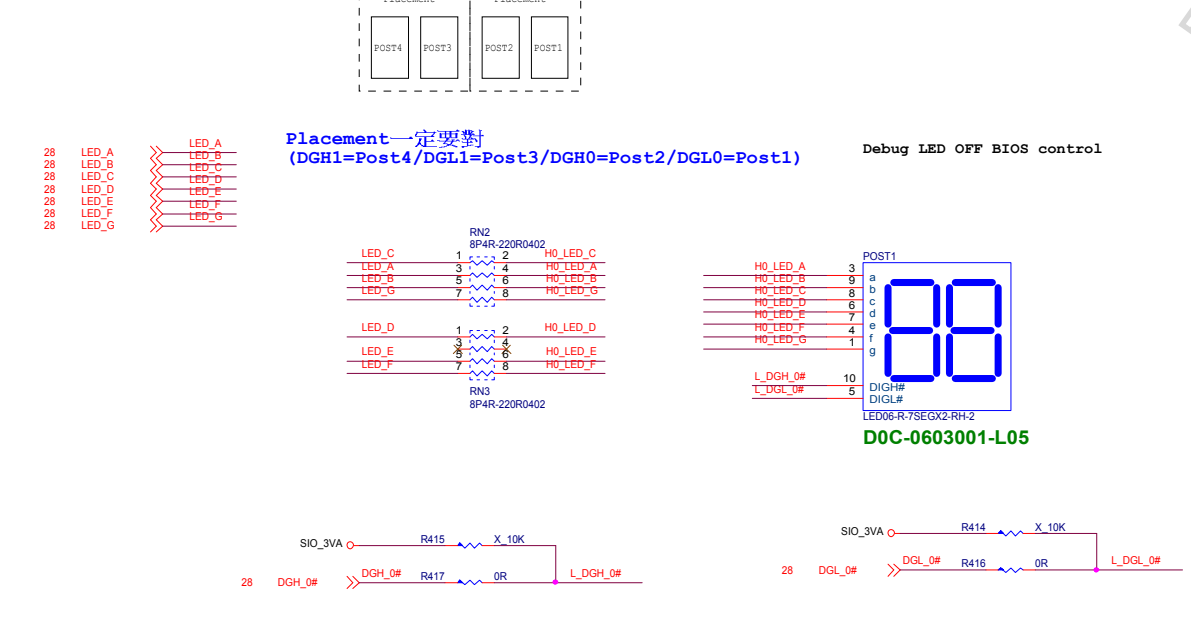
HW Monitor - Voltage



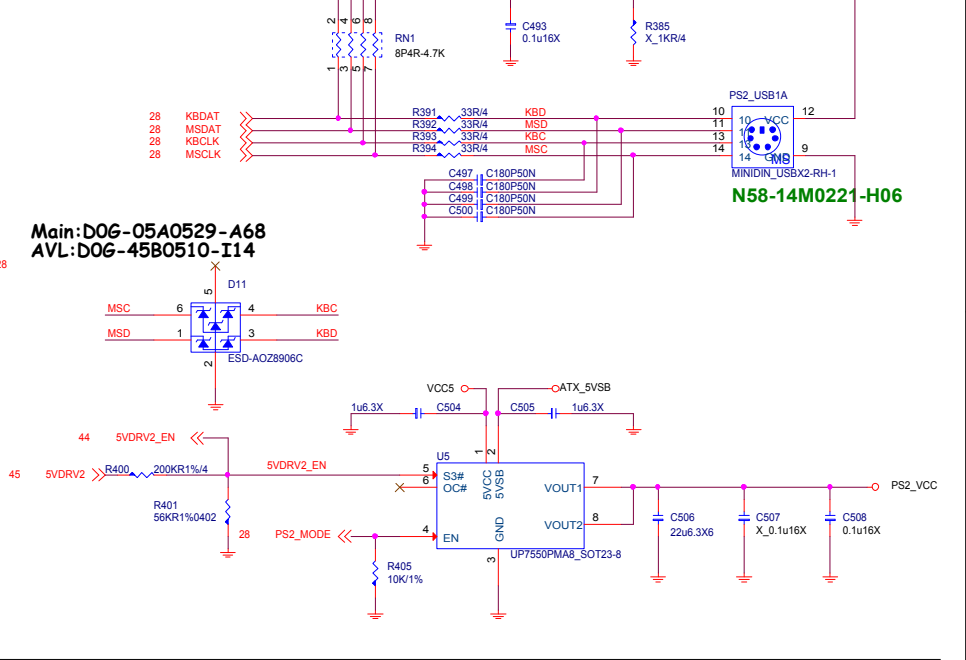
TEMP SENSOR



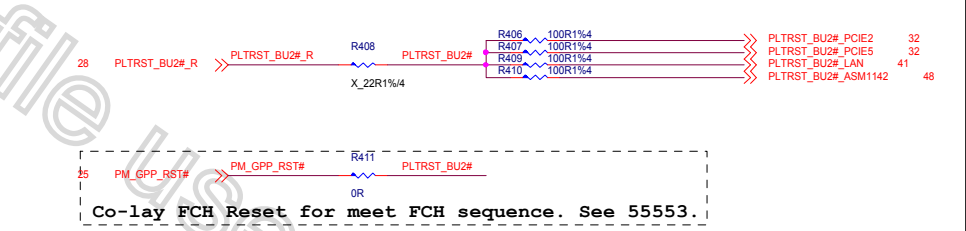
DEBUG LED



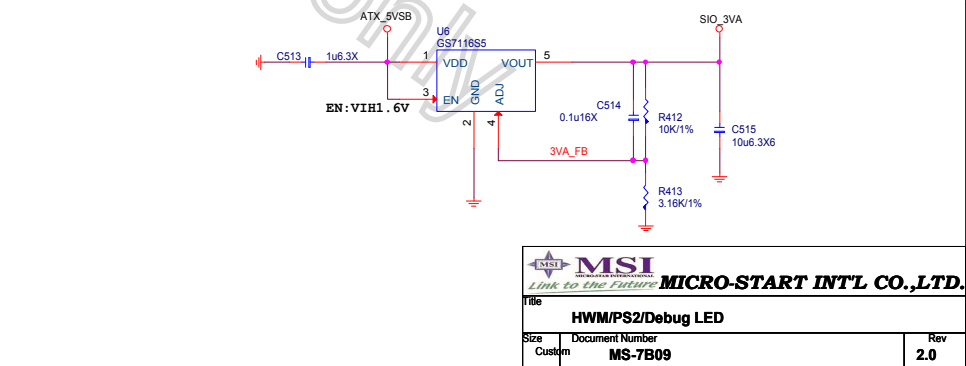
COM PORT



RESET



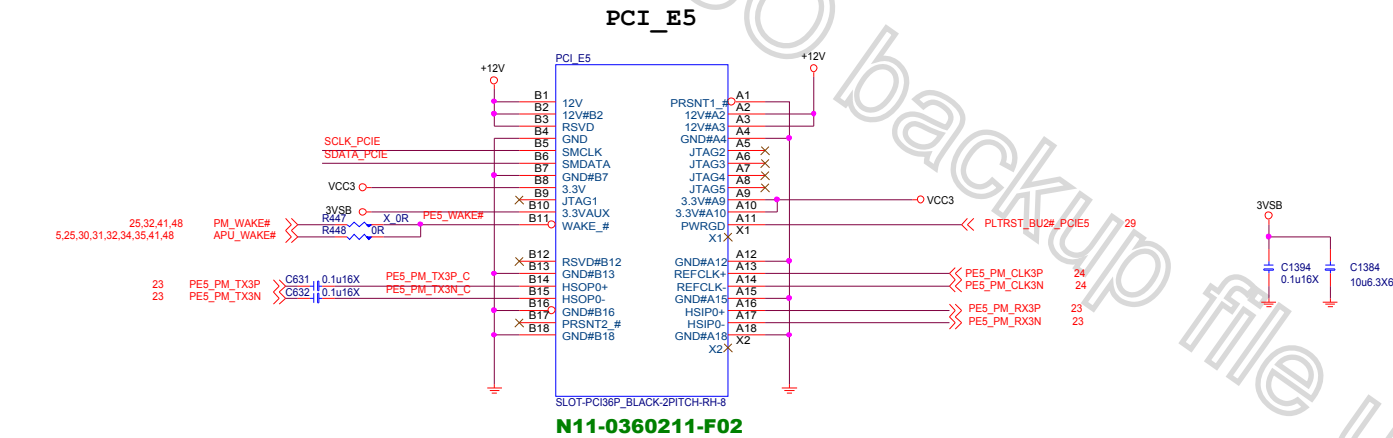
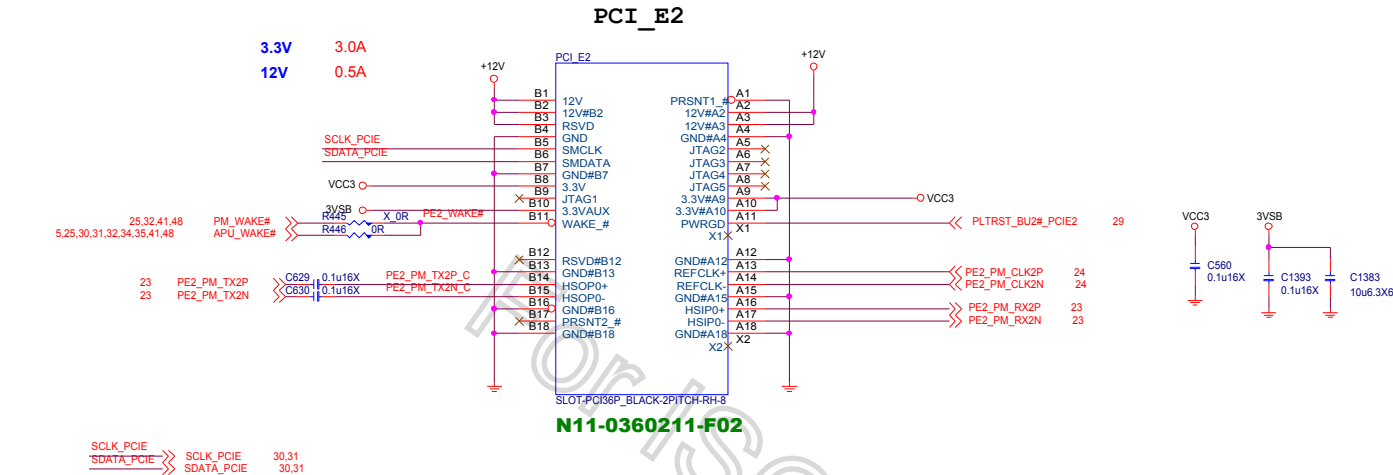
SIO\_3VA








PCIEX1 12V 0.5A  
3.3V weak 375mA



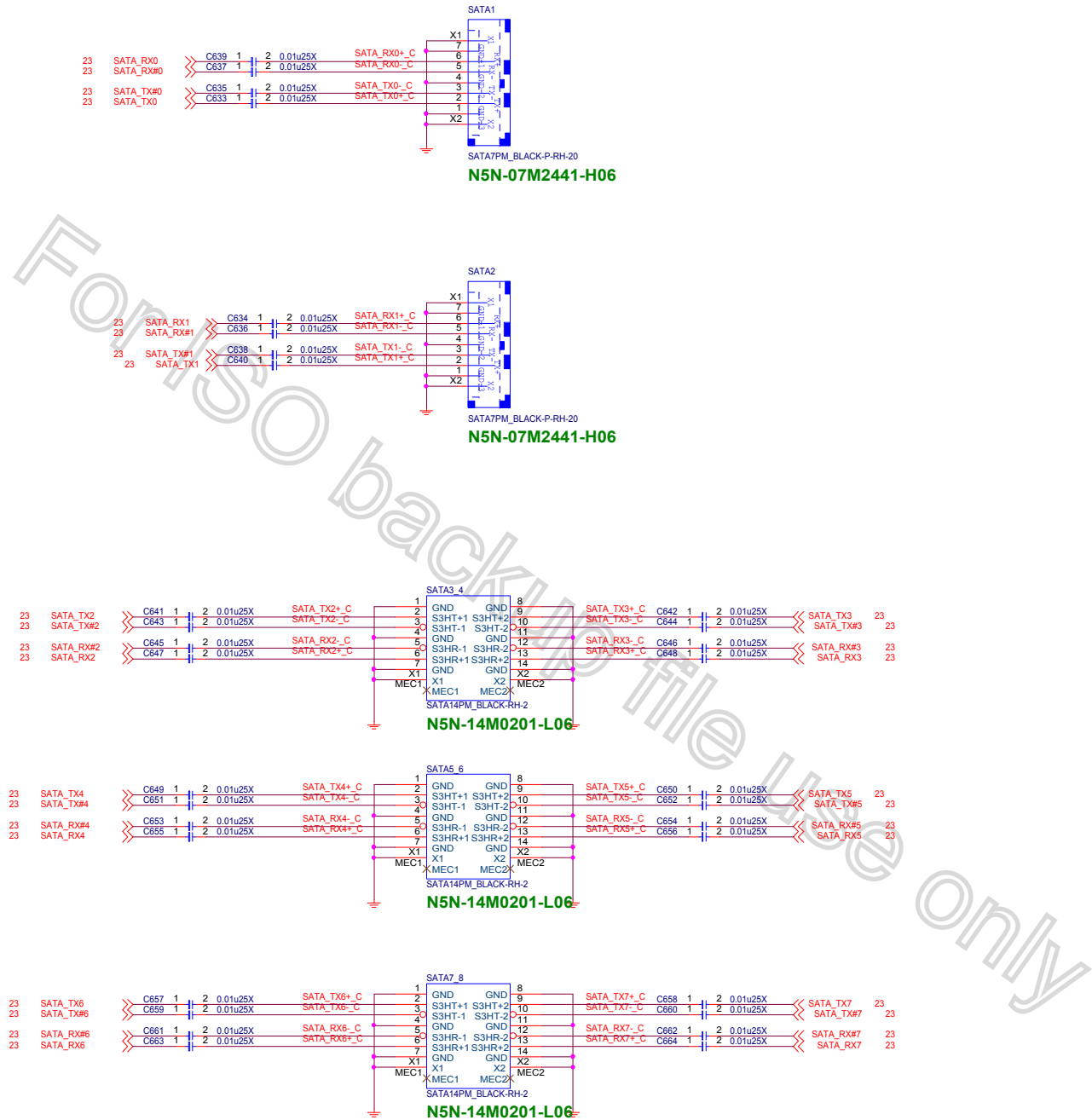
PCI Express X1 slot	
+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A

**MSI**  
Micro-Star International

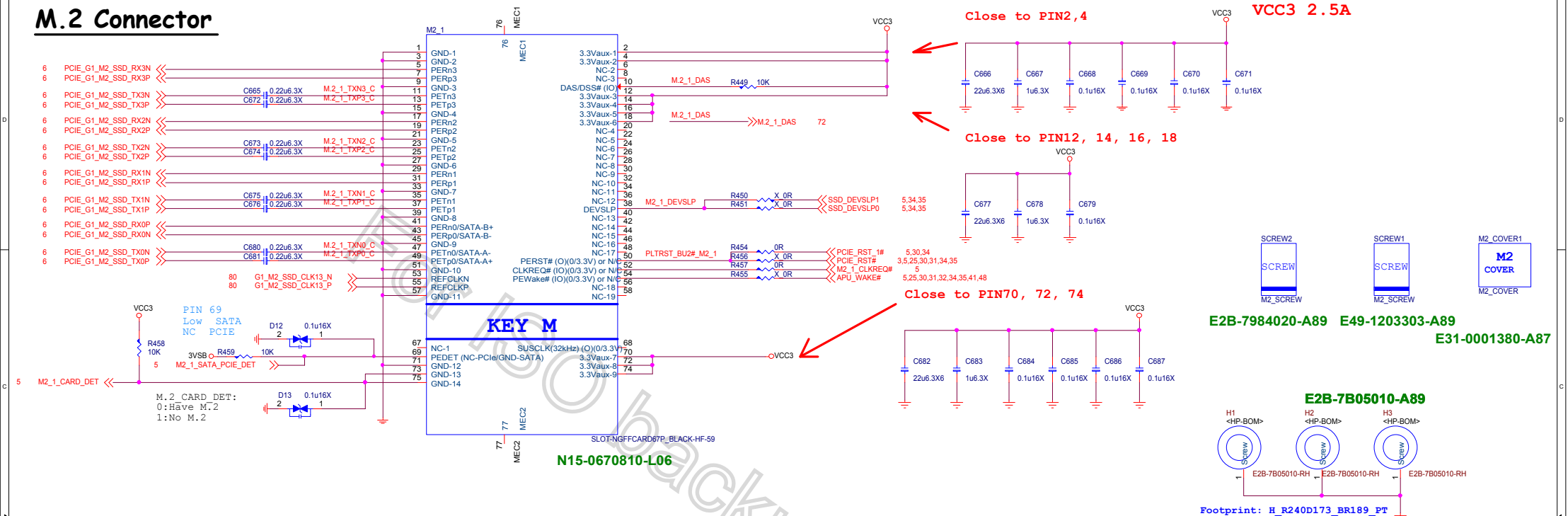
**MICRO-START INT'L CO.,LTD.**

File		MSI X1 & SLOT2&5	
Size	Custom	Document Number	MS-7B09
Date	Thursday, August 10, 2017	Sheet	32 of 87
		Rev	2.0

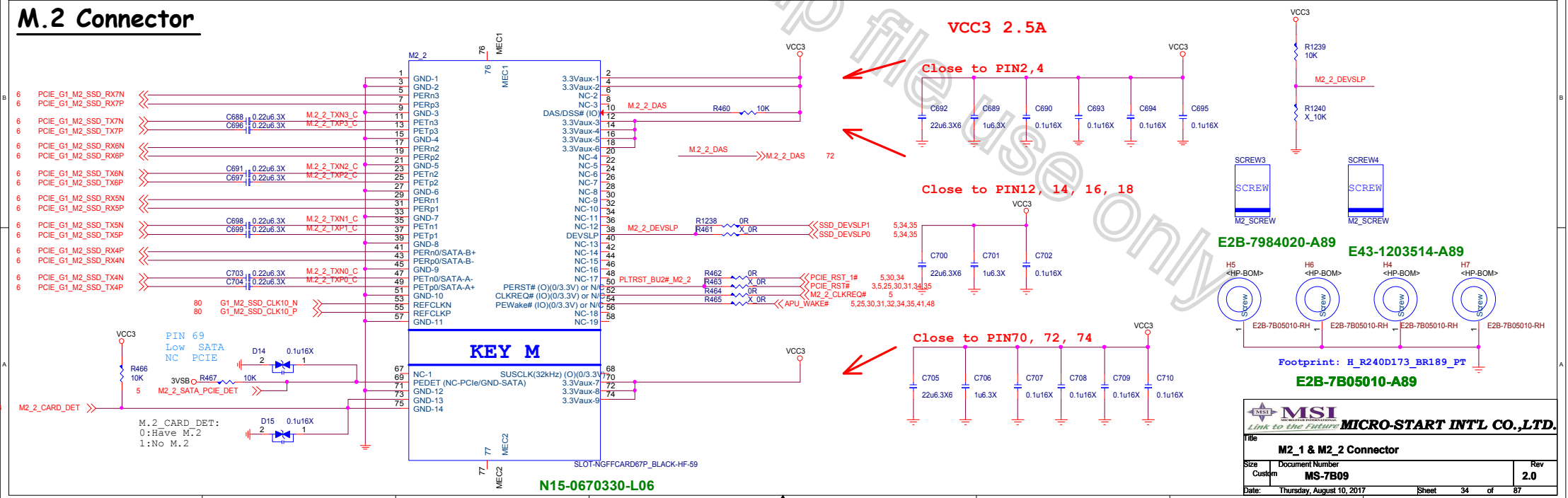
SATA Connector



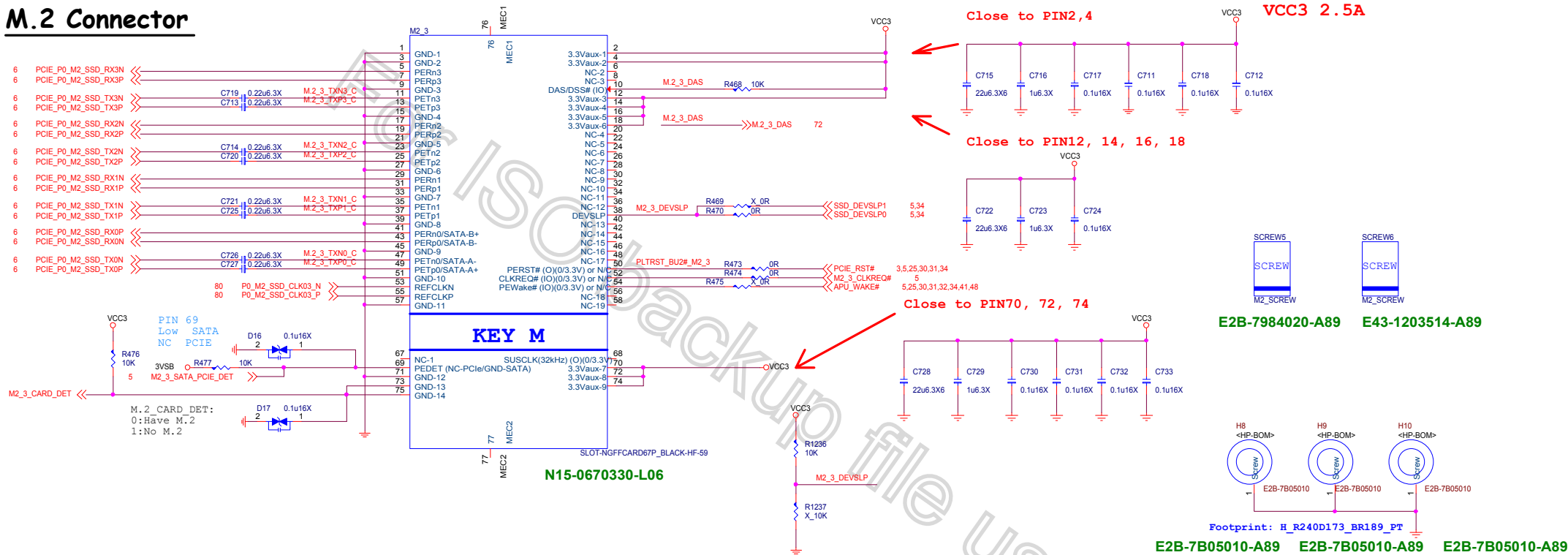
## M.2 Connector

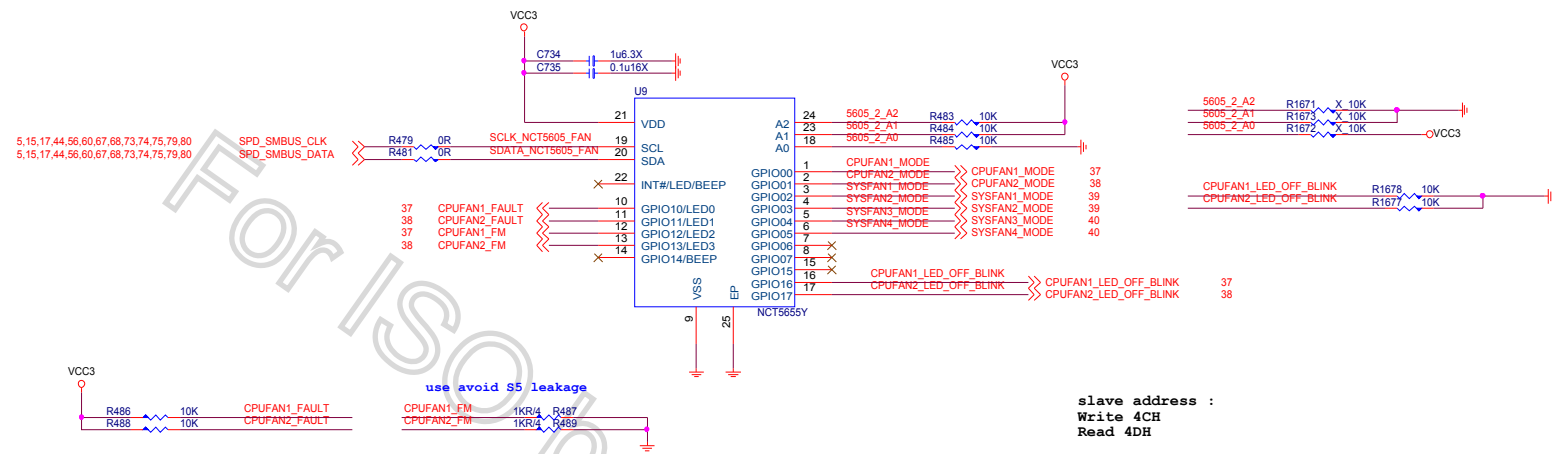


## A.2 Connector



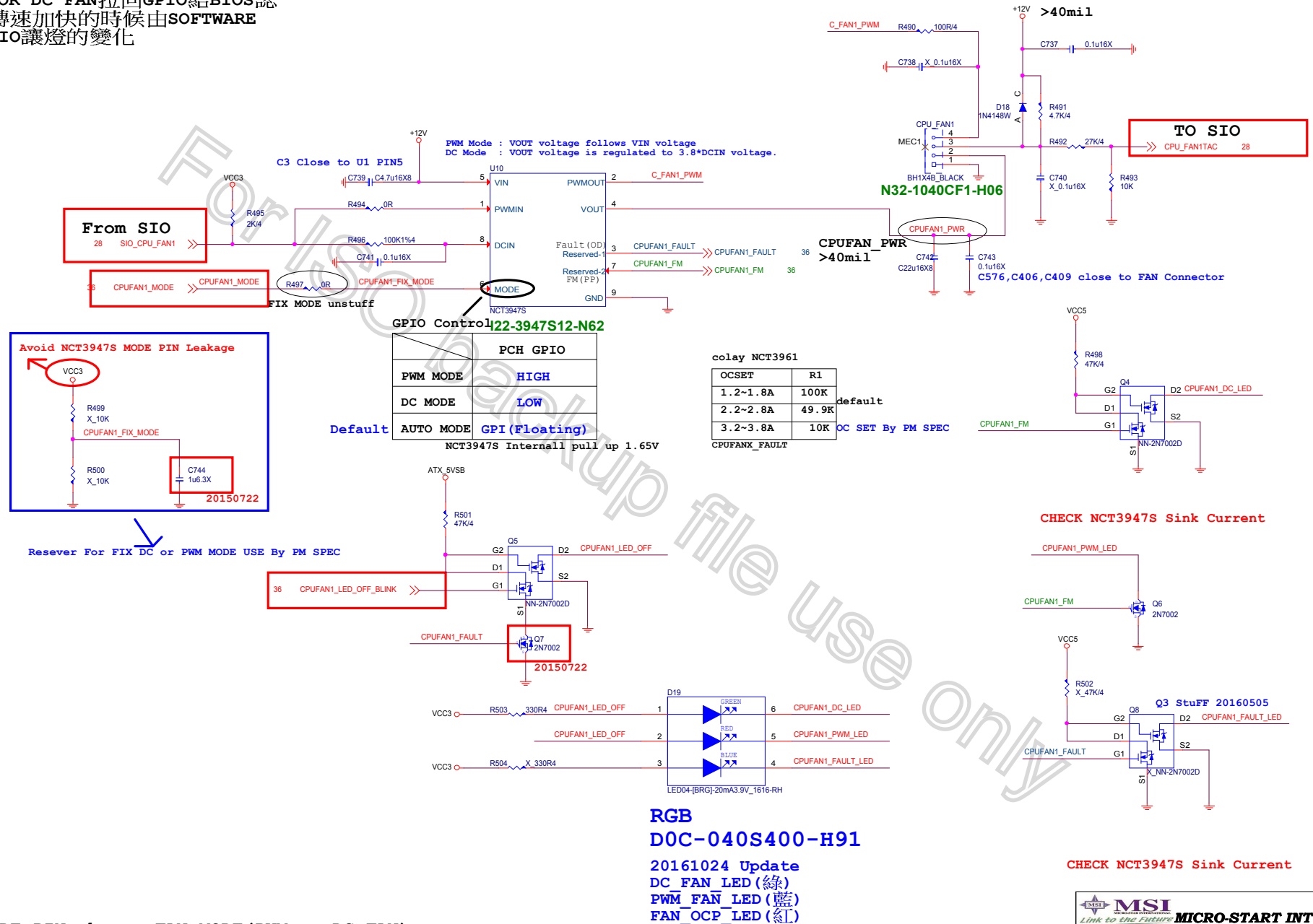
## M.2 Connector





# TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

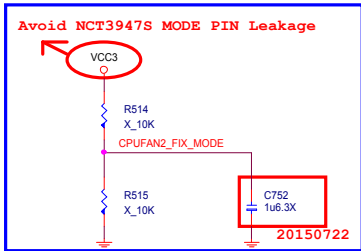
1. PWM/DC/OC LED (現在是改成R/G/B3色LED)
2. GPIO可以由BIOS切換 PWM/DC MODE
3. OCP拉回GPIO給BIOS認
4. PWM OR DC FAN拉回GPIO給BIOS認
5. FAN轉速加快的時候由SOFTWARE控制GPIO讓燈的變化



1. MODE : USE MODE PIN change FAN MODE (PWM or DC FAN)
2. FAULT : USE FAULT PIN Triger OVT/OC Protection, LOW Atcive (Reserve NEW IC)
3. FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information (Reserve NEW IC)

1. PWM/DC/OCF LED (現在是改成R/G/B3色LED)
2. GPIO可以由BIOS切換 PWM/DC MODE
3. OCF拉回GPIO給BIOS認
4. PWM OR DC FAN拉回GPIO給BIOS認
5. FAN轉速加快的時候由SOFTWARE  
控制GPIO讓燈的變化

1. PWM/DC/OCF LED (現在是改成R/G/B3色LED)
2. GPIO可以由BIOS切換 PWM/DC MODE
3. OCF拉回GPIO給BIOS認
4. PWM OR DC FAN拉回GPIO給BIOS認
5. FAN轉速加快的時候由SOFTWARE控制GPIO讓燈的變化



Resever For FIX DC or PWM MODE USE By PM SPEC

GPIO Control		I22-3947S12-N62
	PCH GPIO	
PWM MODE	HIGH	
DC MODE	LOW	
AUTO MODE	GPI(Floating)	

NCT3947S Internall pull up 1.65V

NCT3947S Internall pull up 1.65V

```
colay NCT3961
```

OCSET	R1
1.2~1.8A	100K
2.2~2.8A	49.9K
3.2~3.8A	10K

CPUFANX FAULT

OC SET By PM SPEC

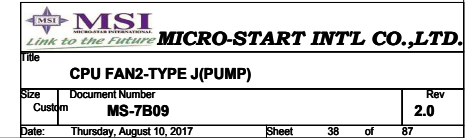
### CHECK NCT3947S Sink Current

CPUFAN2\_PWM\_LED

CPUFAN2\_FM

Q11  
2N7002

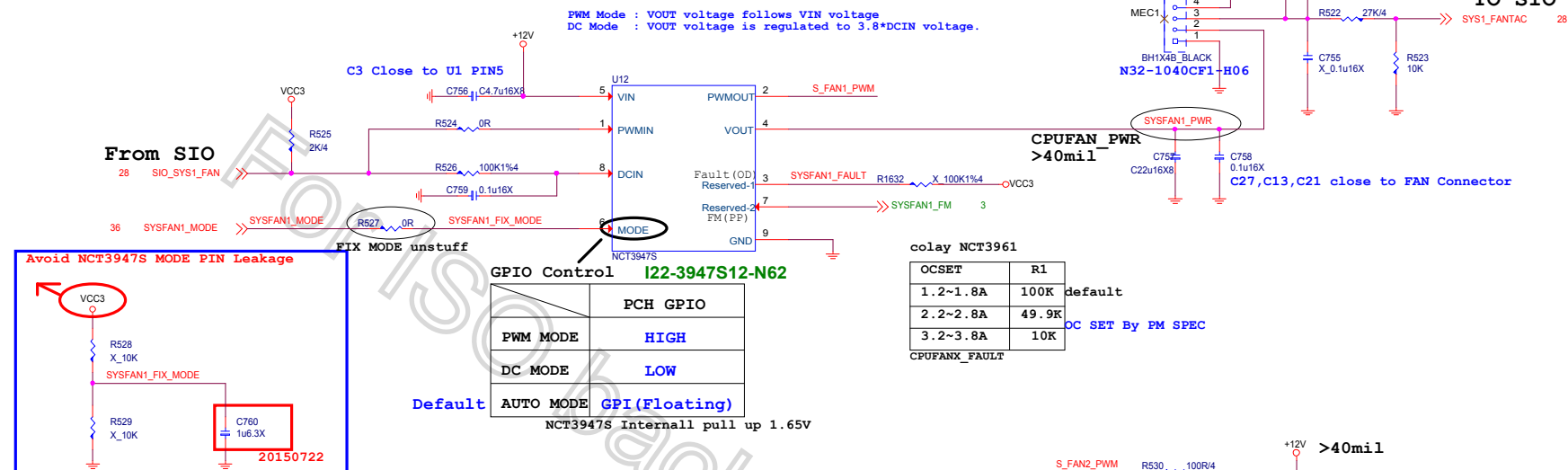
CHECK NCT3947S Sink Current



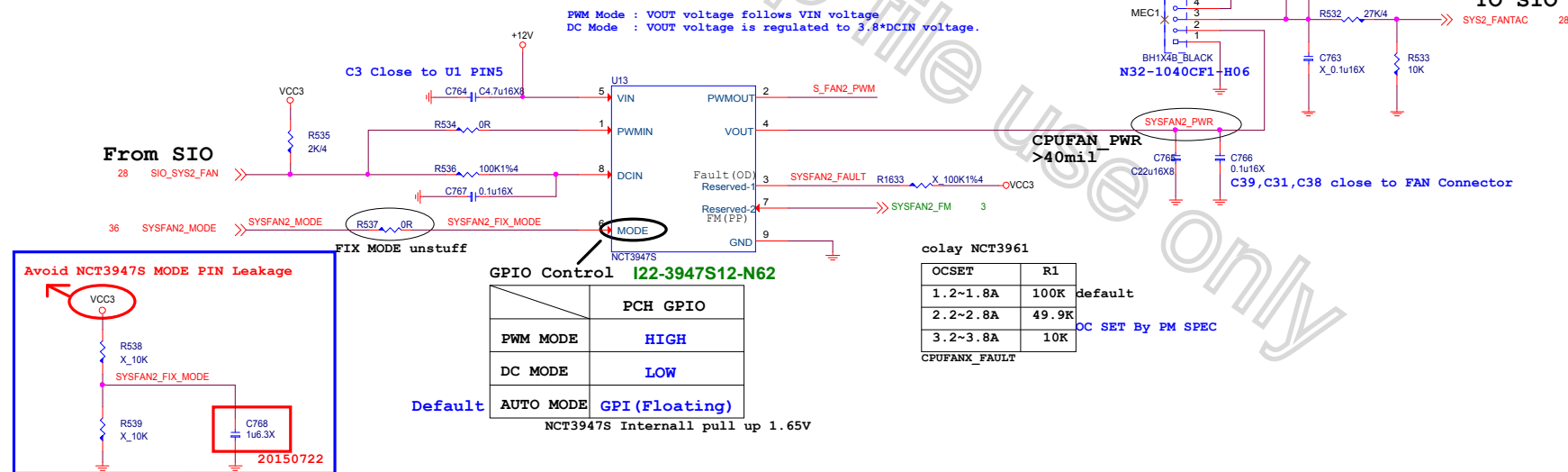
- 1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN) FAN\_OCP\_LED(紅)  
2.FAULT : USE FAULT PIN Triger OVT/OCP Protection,LOW Atcive (Reserve NEW IC)  
3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

# TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1. Mode GPIO BIOS can switch PWM/DC Mode
2. FM:BIOS can read FAN PWM/DC Mode



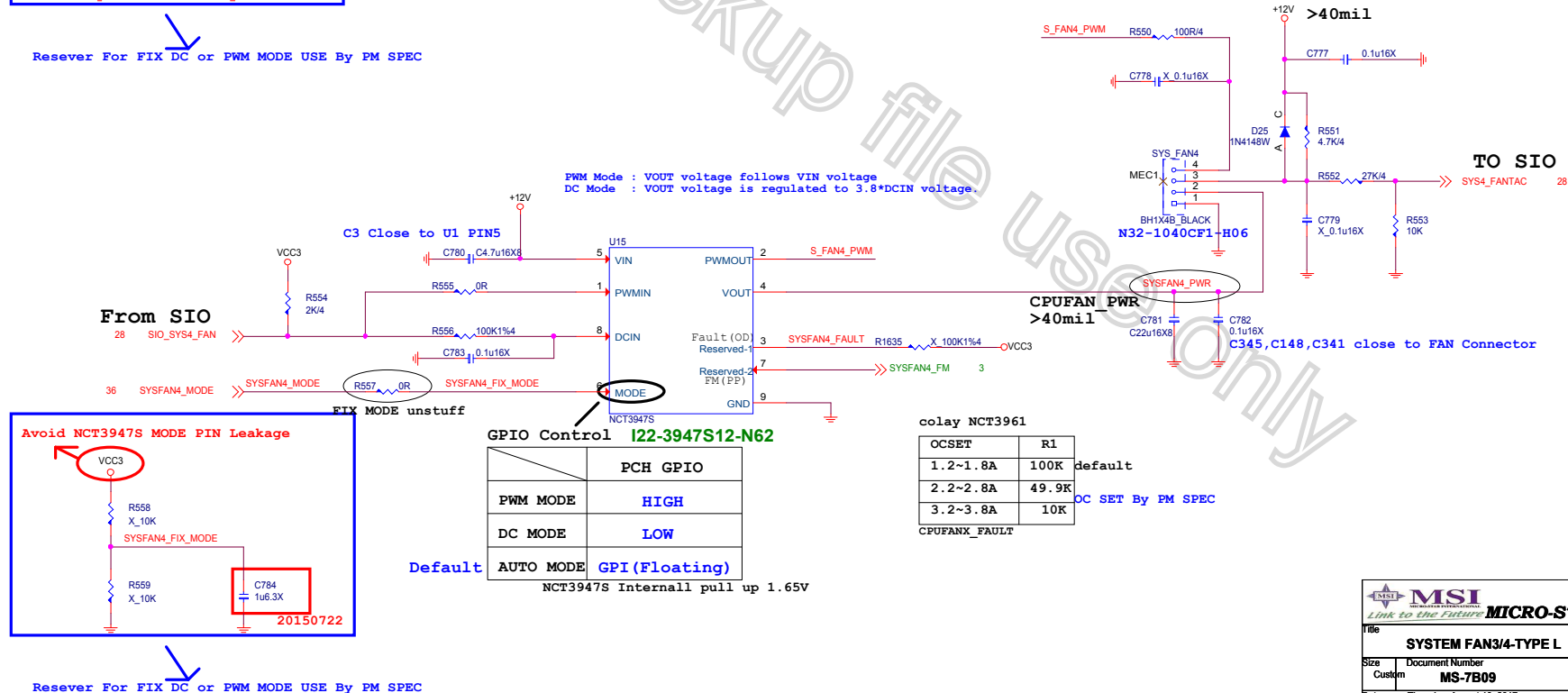
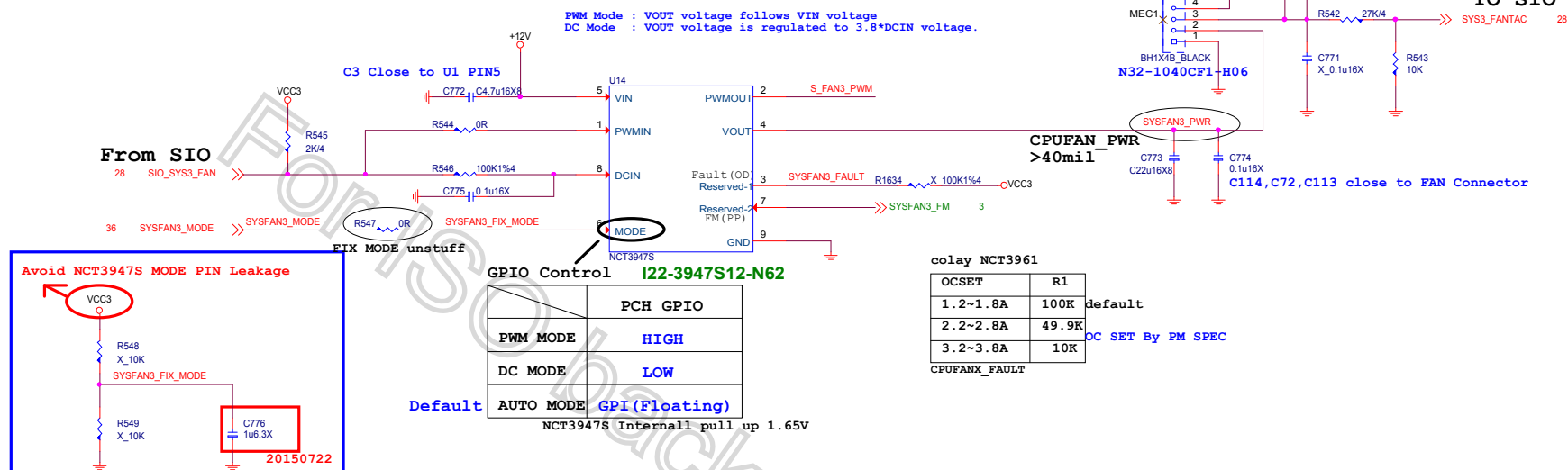
Resever For FIX DC or PWM MODE USE By PM SPEC



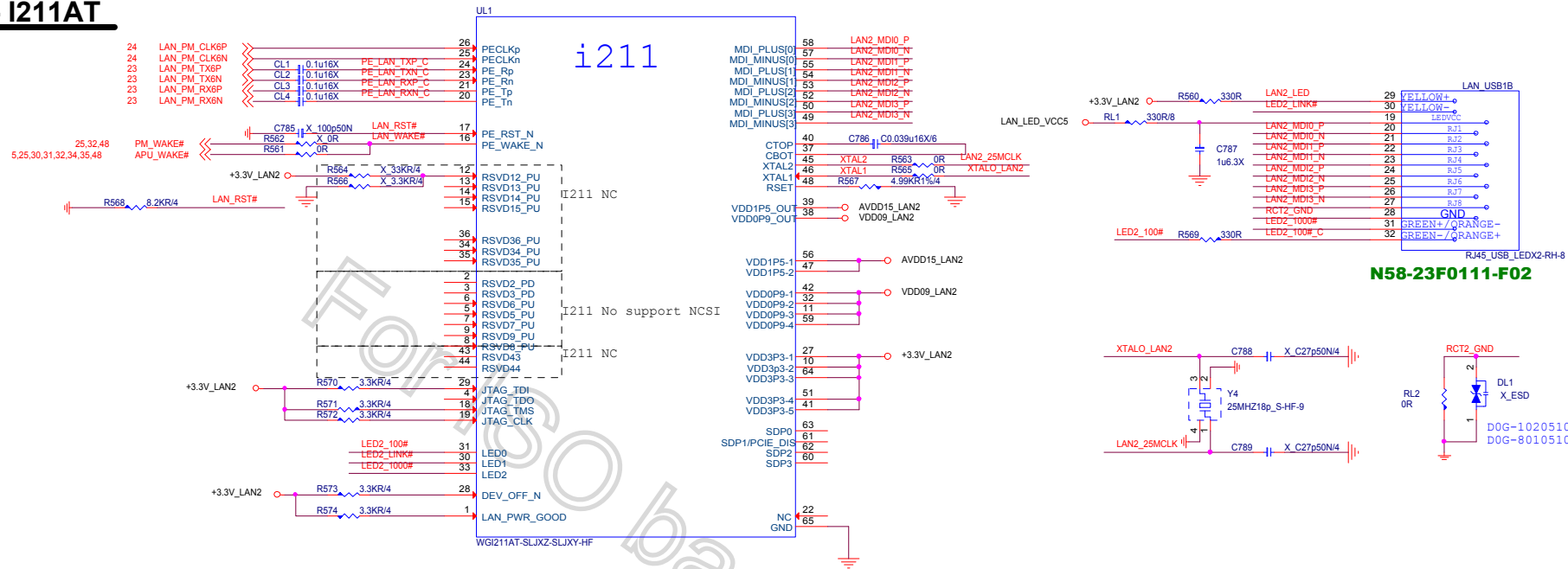
Resever For FIX DC or PWM MODE USE By PM SPEC

# TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1. Mode GPIO BIOS can switch PWM/DC Mode
2. FM:BIOS can read FAN PWM/DC Mode

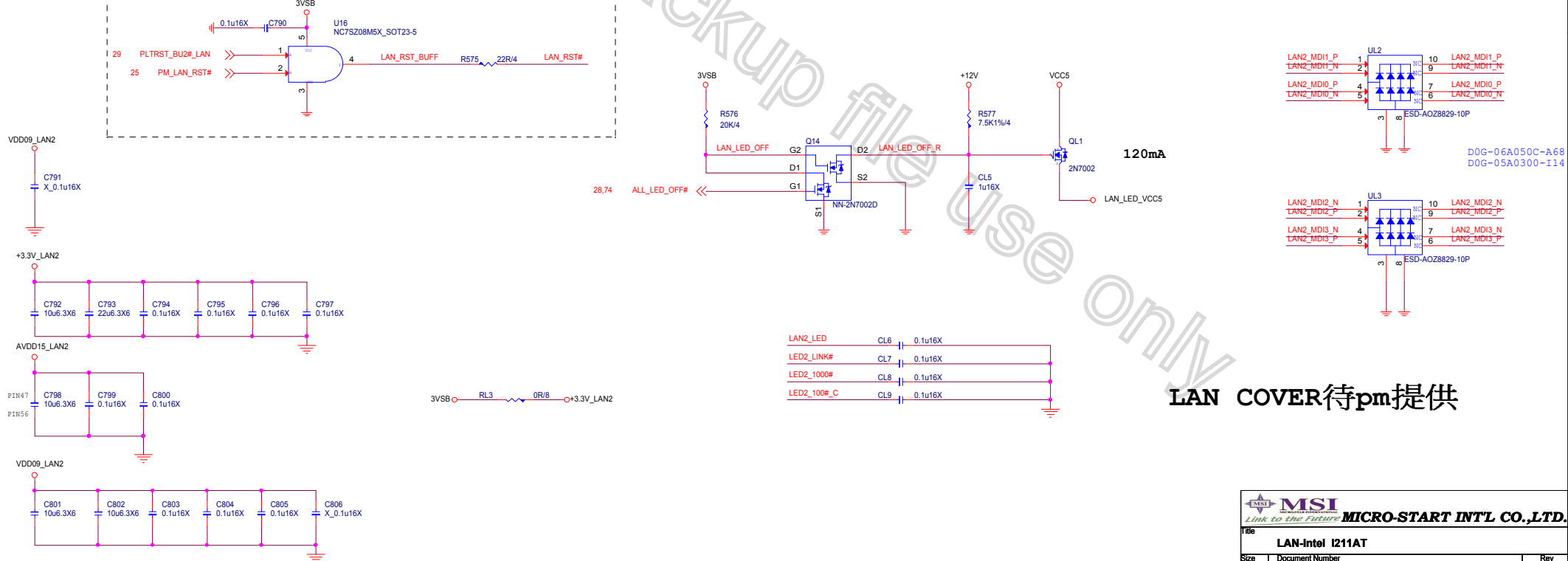


**LAN-- I211AT**



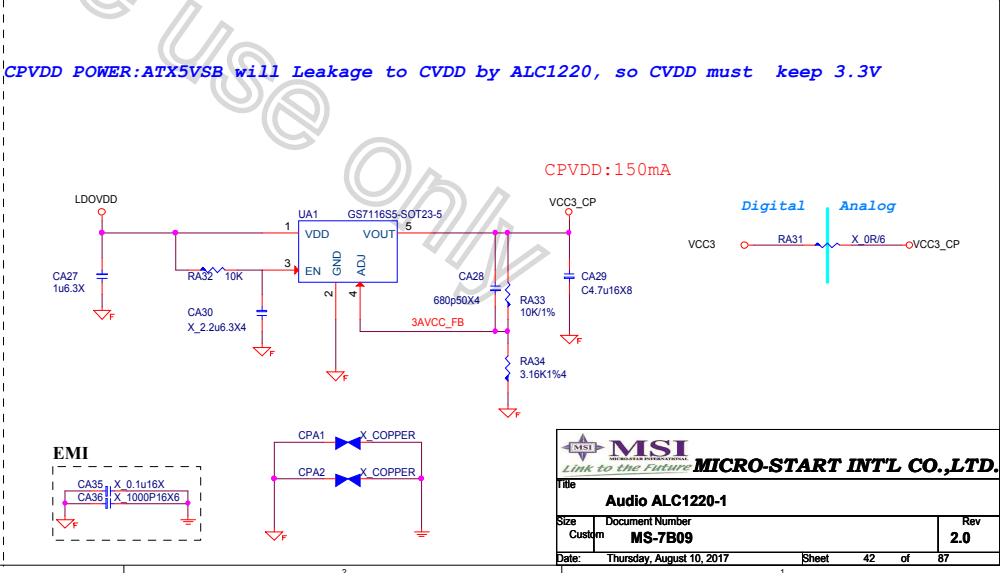
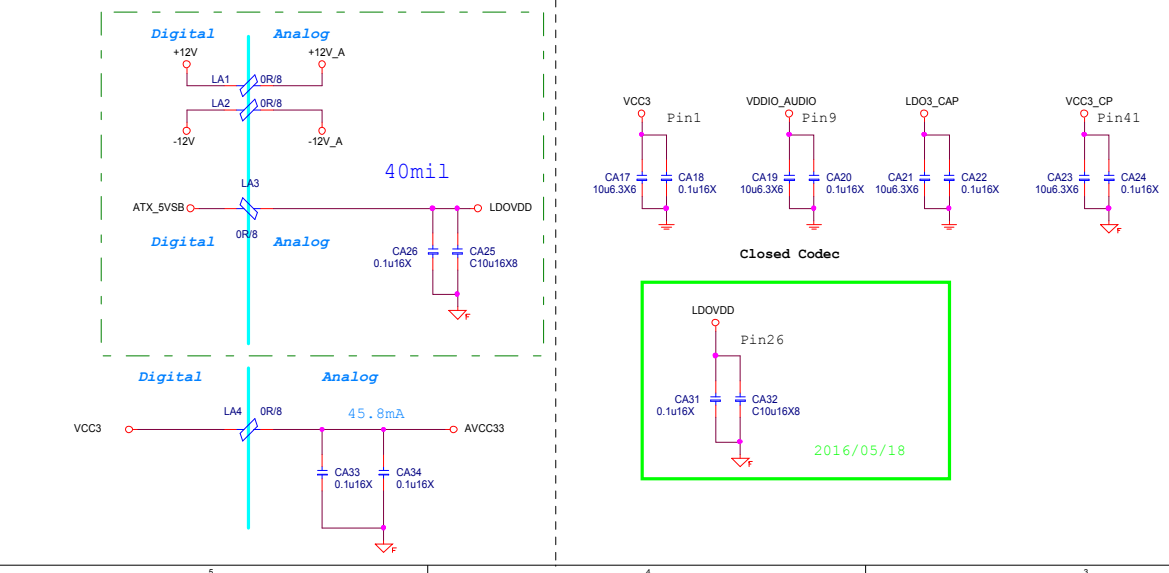
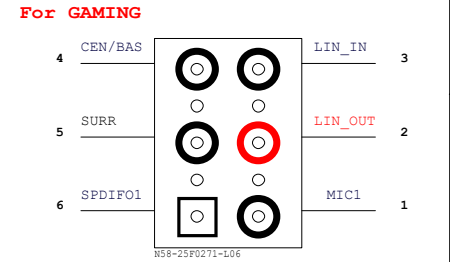
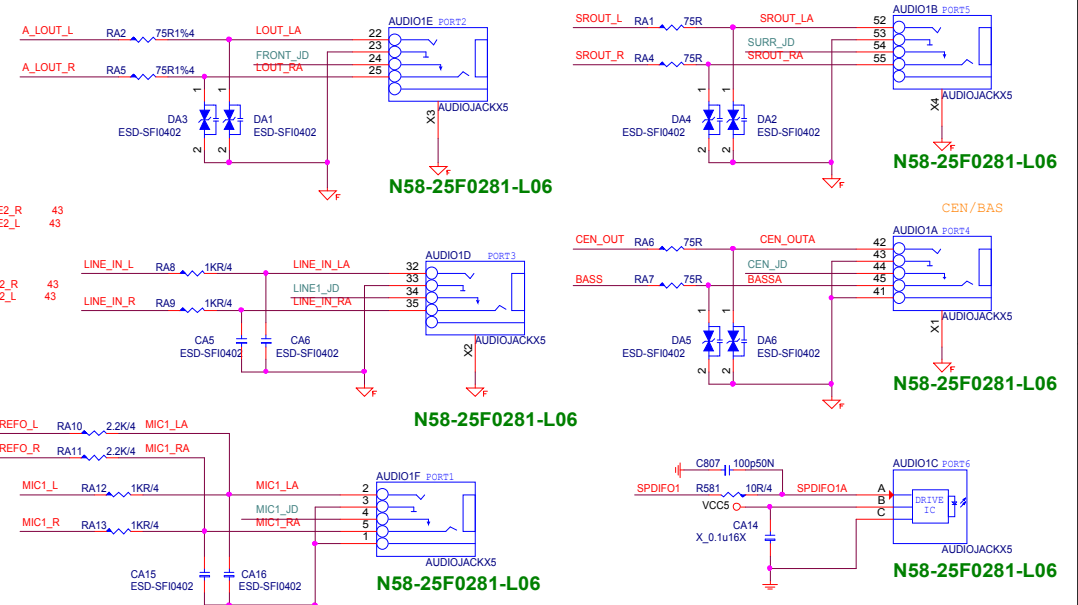
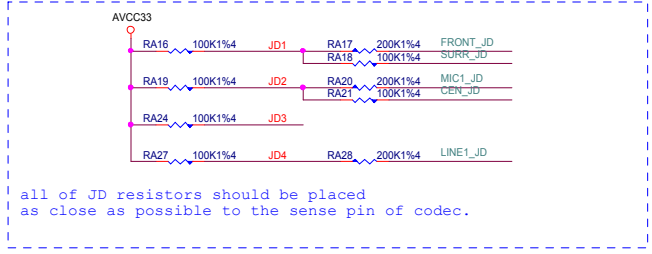
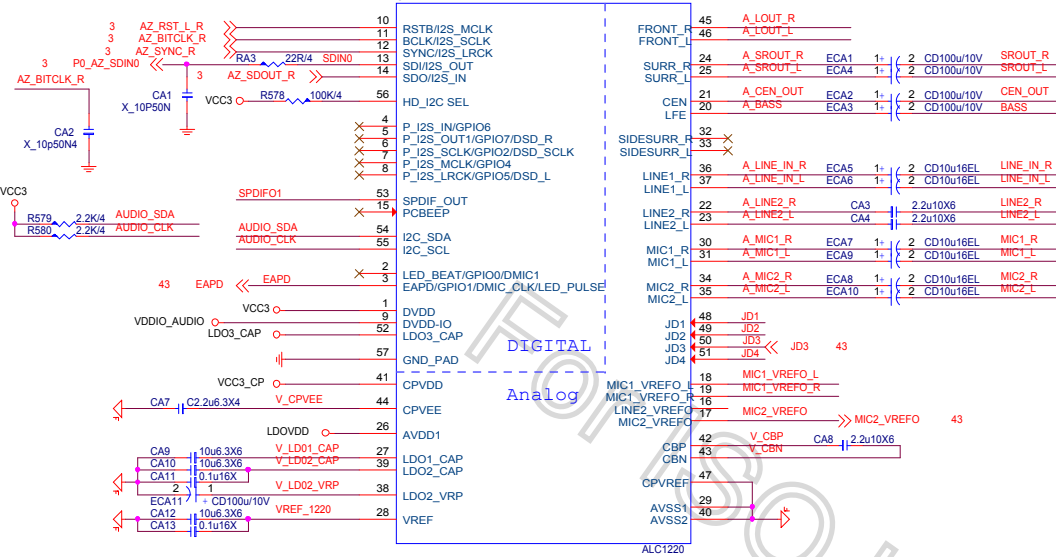
2016.07.21 Add

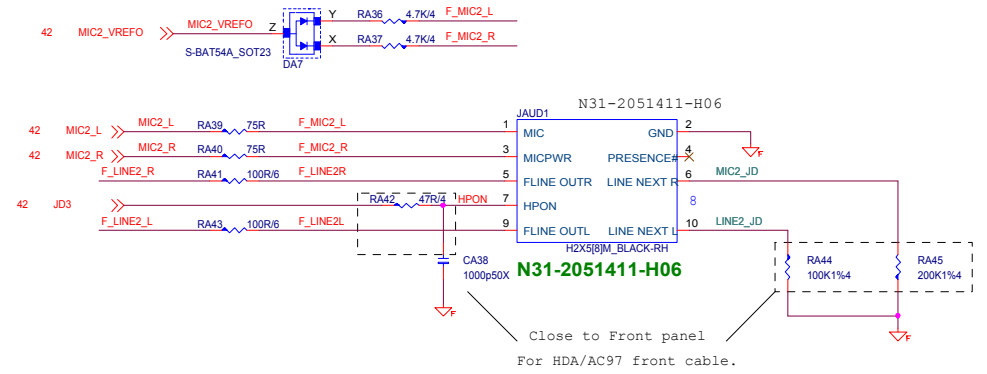
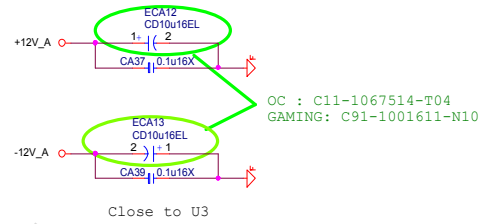
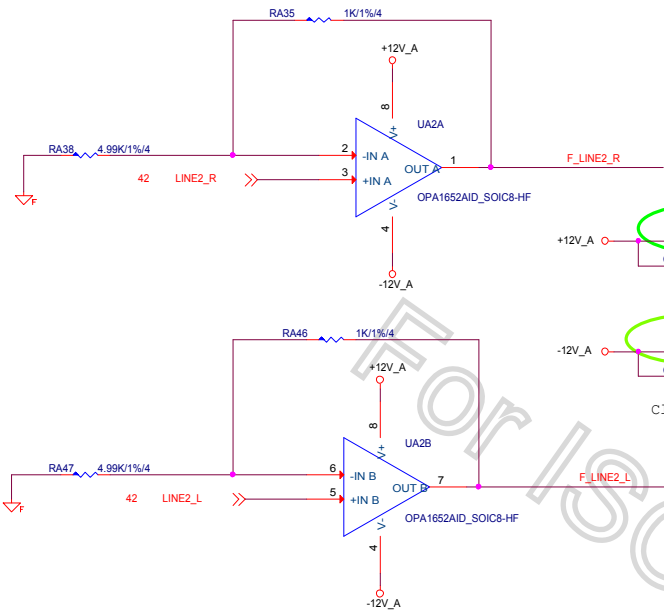
## Disable LAN Function



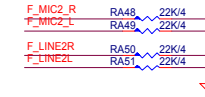
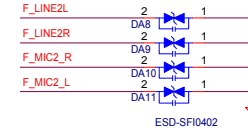
LAN COVER待pm提供

ALC1220



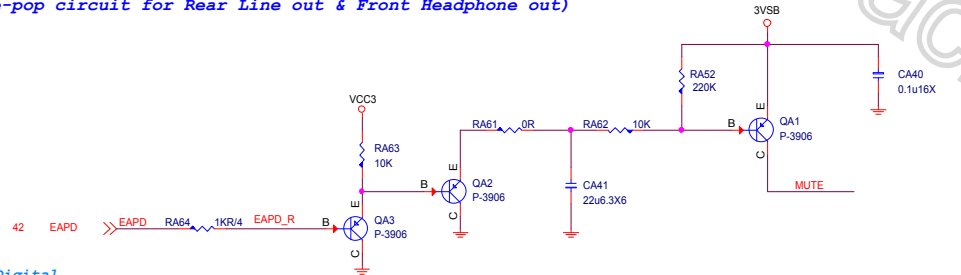


Close to Jack  
**ESD protect**  
 D0G-2950500-SI0  
 D0G-3010510-I05



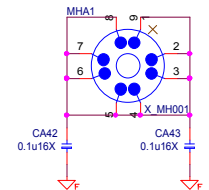
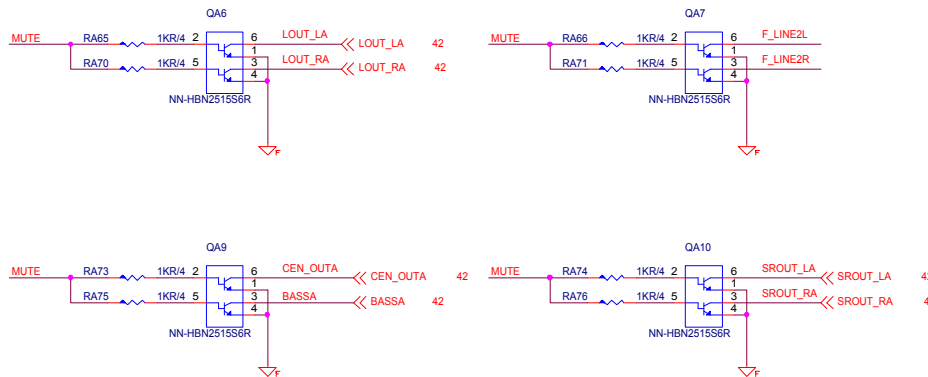
#### Rear Line OUT De-POP circuit

(De-pop circuit for Rear Line out & Front Headphone out)



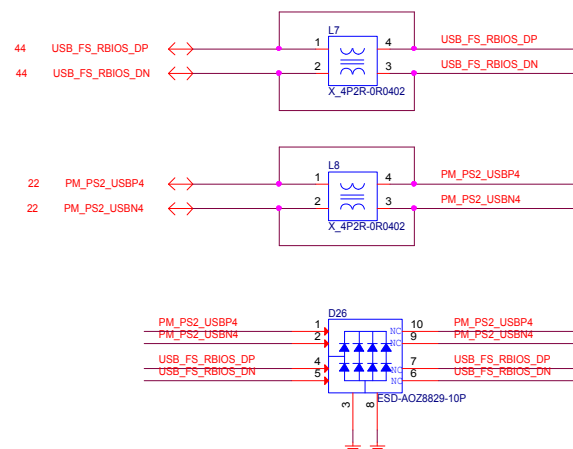
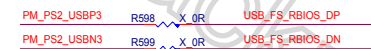
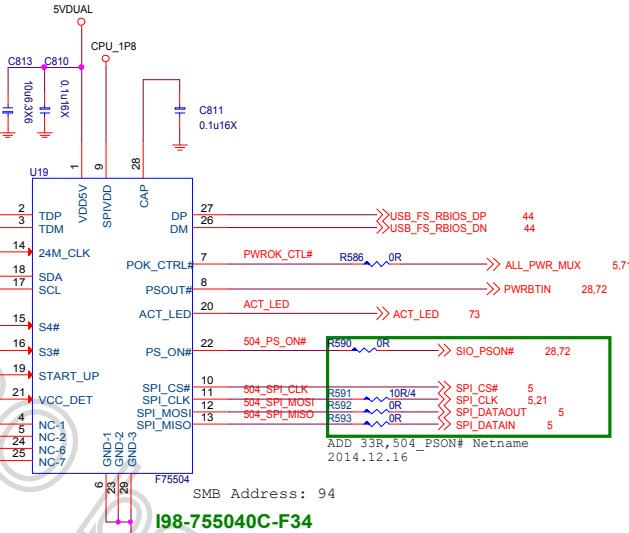
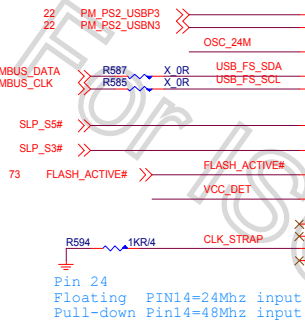
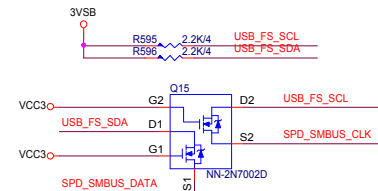
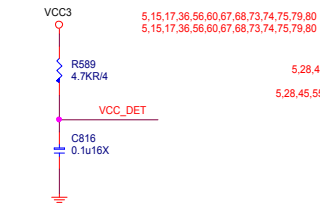
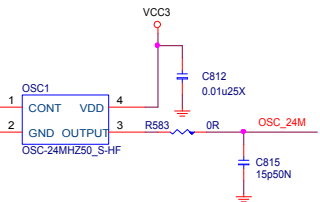
Digital

Analog



# USB Flash BIOS

Host USB connector

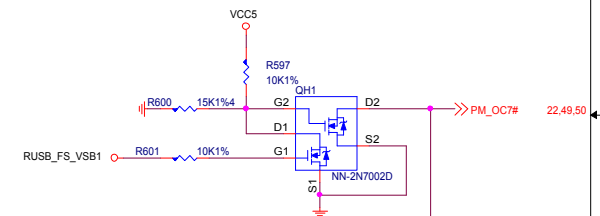
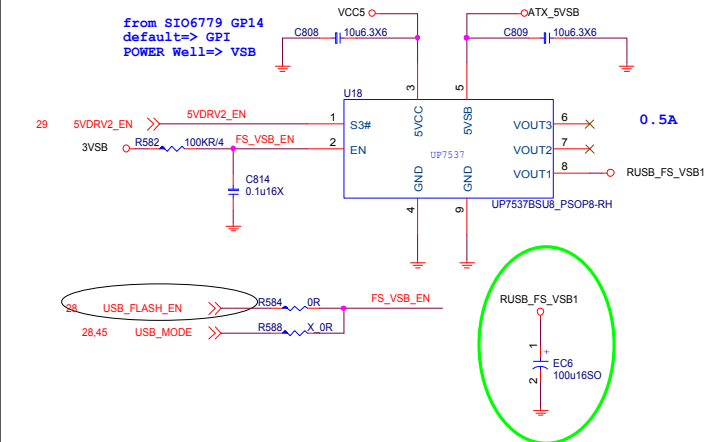


ESD close to connector.  
(use usb3.0 ESD for eye diagram)

Reserved for when F75501 Hotkey device fail use

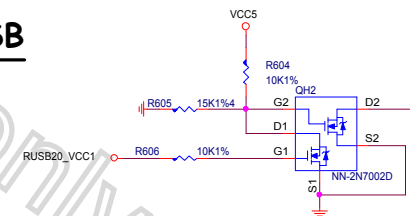
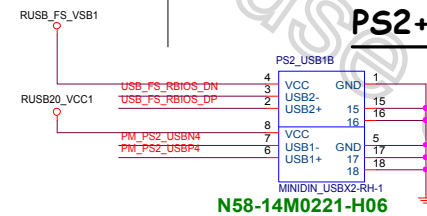
\* All close to Front IO side

## REAR Flash BIOS USB PORT 9



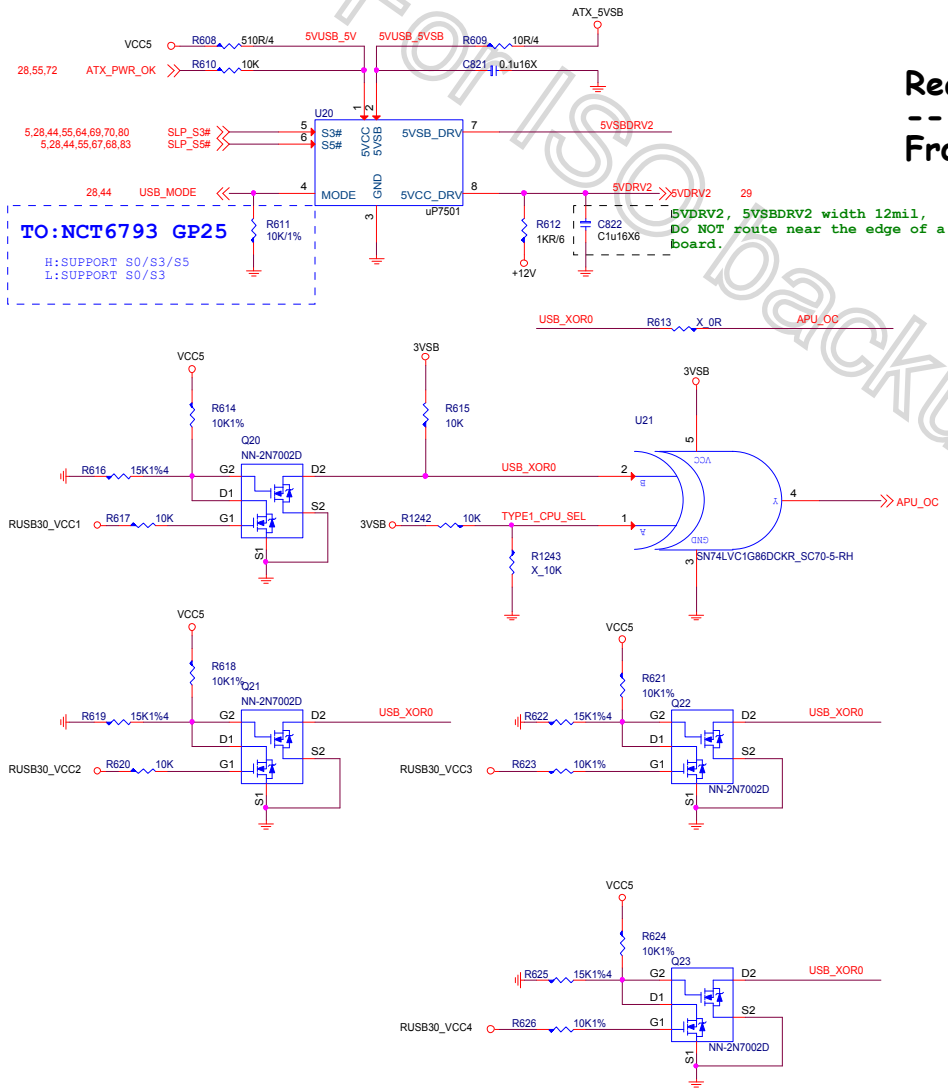
OC# signal connect to SB OC pin.

USB Connector power come from UP7537 provide(USB Hotkey Connector same)

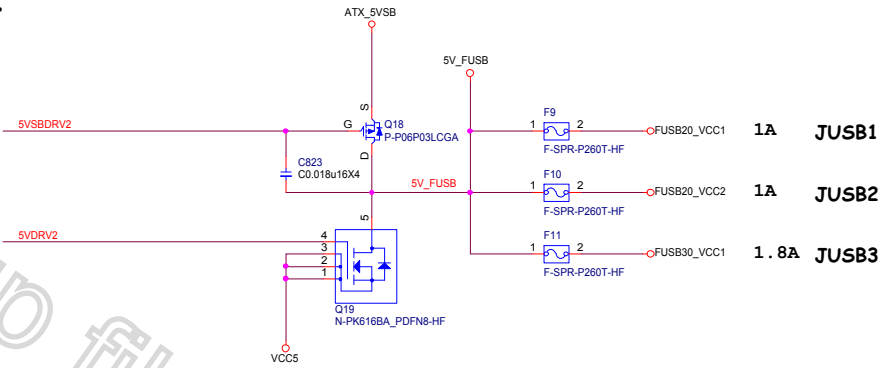
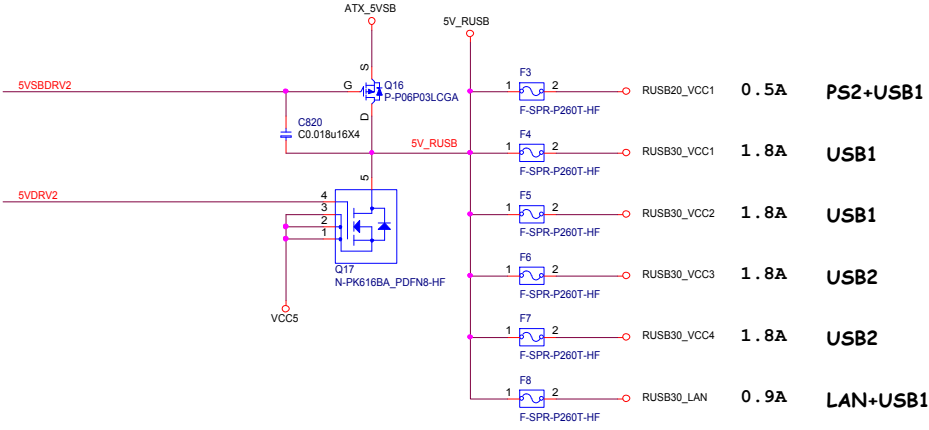


OC# signal connect to SB OC pin.

USB Power

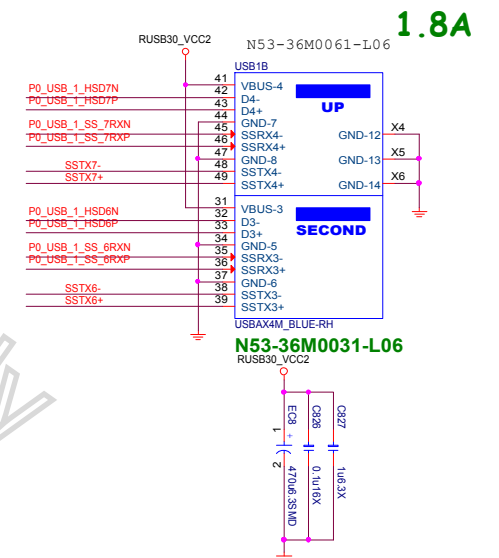
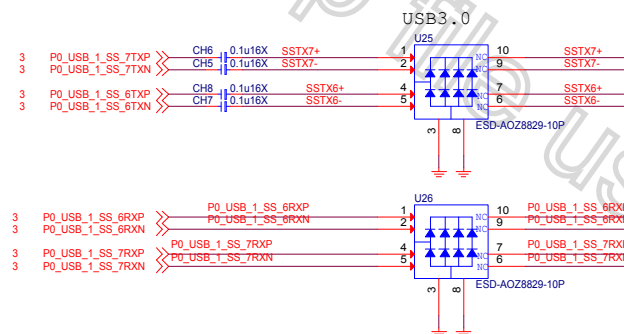
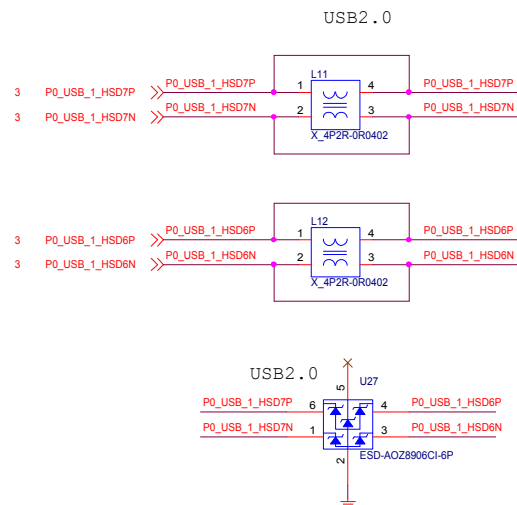
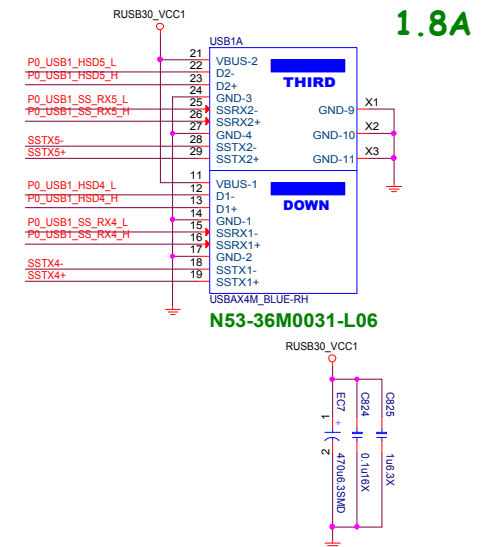
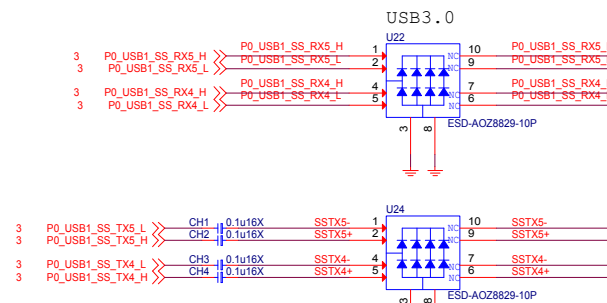
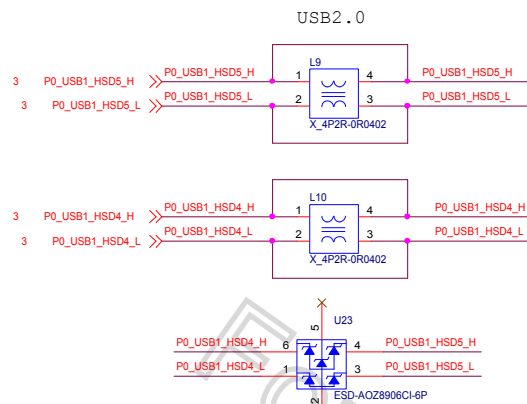


Rear  
Front

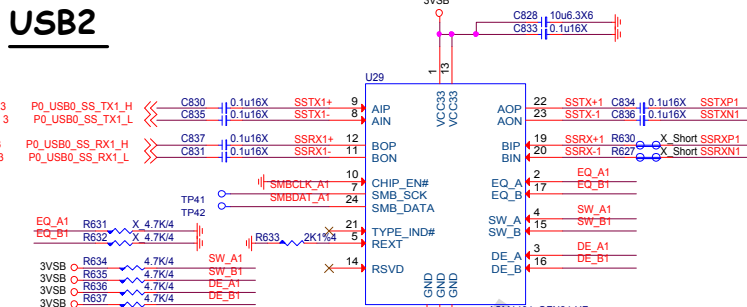


	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

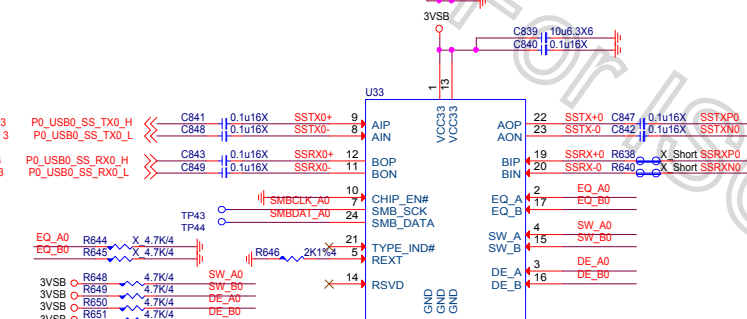
## USB1



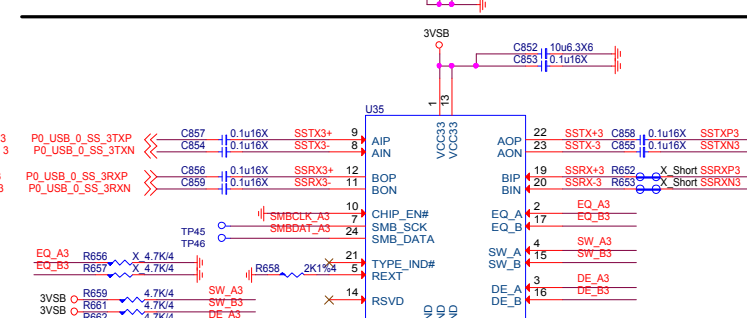
# USB2



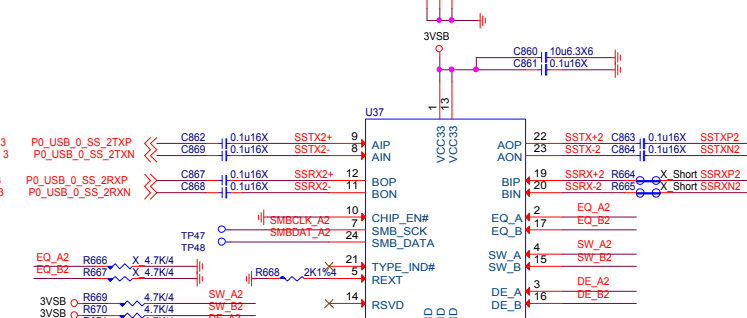
I9B-M14640C-AD0



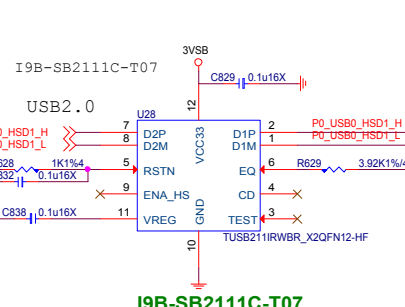
I9B-M14640C-AD0



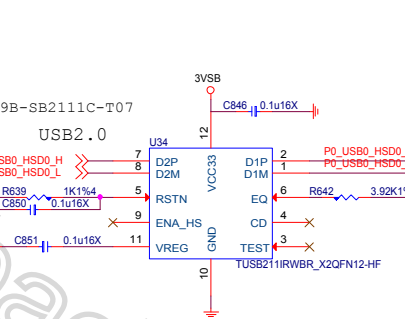
I9B-M14640C-AD0



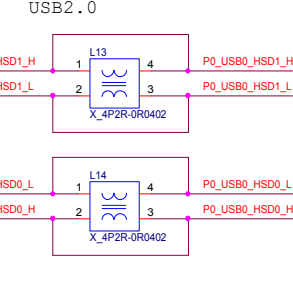
I9B-M14640C-AD0



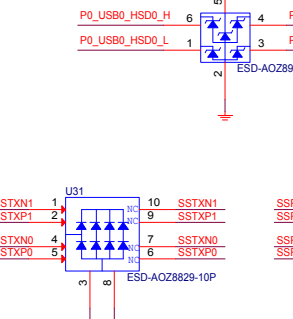
I9B-SB2111C-T07



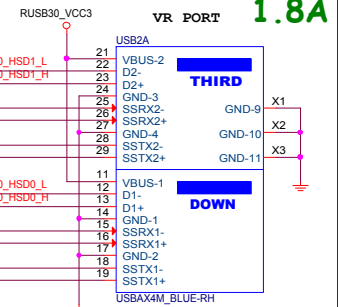
I9B-SB2111C-T07



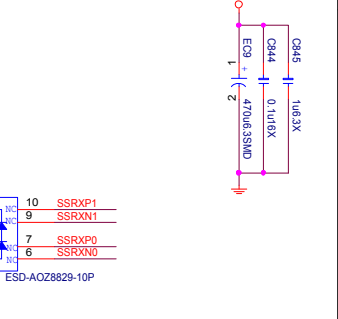
USB2.0



USB2.0



VR PORT



VR PORT

1.8A

1.8A

Use pure PCIE must provide CLK

Minimum gap should be greater of  
>15mil with other signal.

Chip to Connector  
1.5 inch.

Layout Guide:

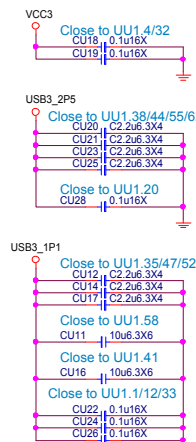
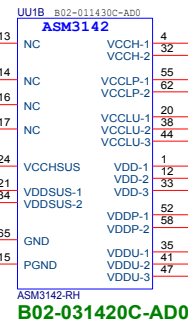
- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole < 2

Power Consumption

	3.3V	3.3VSUS	2.5V	1.1V	1.1VSUS	Unit
ASM3142	TBD	TBD	TBD	TBD	TBD	mA
ASM2142	4	9	220	470	10	mA

X0/XI (95hm-Diff.Spacing 30mil)  
UREXT,PEUREXT(W/S): 10/7  
OCIA,OCIB,PPONA,PPONB(W/S): 5/6

SMD Crystal use 3225 size  
M:D04-0900900-SC6  
S:D04-0901100-T16  
S:D04-0901200-F07



2016.07.21 Add

Disable ASM1142 Function

### ASM3142 1.1v Core Power

### ASM3142 1.1v Suspend Power

### EEPROM

### M31-25L1022-M24

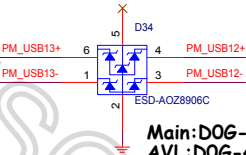
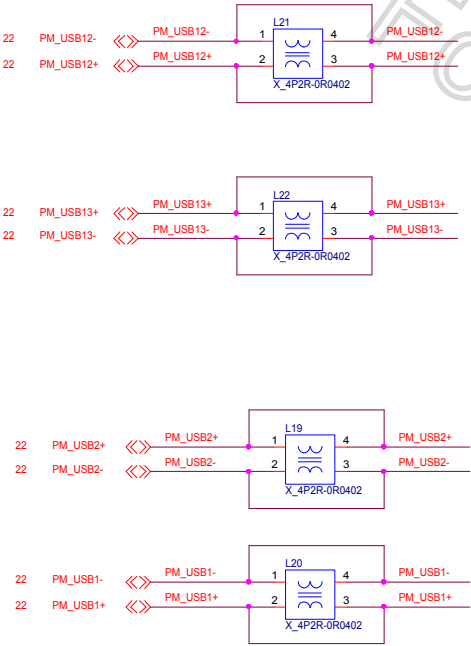
M:M31-25L1022-M24 (1M)  
S:M31-25X2023-W03 (2M)

MSI  
Link to the Future  
MICRO-START INTL CO.,LTD.

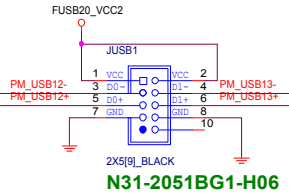
Title			USB3.1 ASM1142-1		
Size	Document Number	Rev			
Custom	MS-7B09	2.0			
Date:	Thursday, August 10, 2017	Sheet	48	of	87



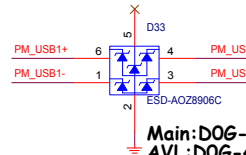
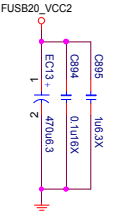
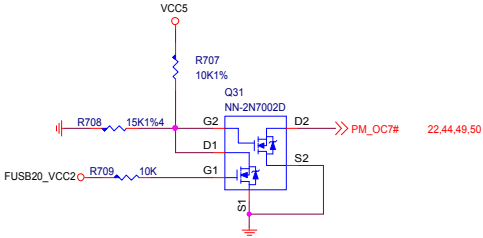
JUSB1+JUAB2



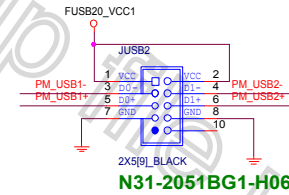
Main:D0G-05A0529-A68  
AVL:D0G-45B0510-I14



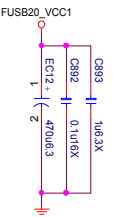
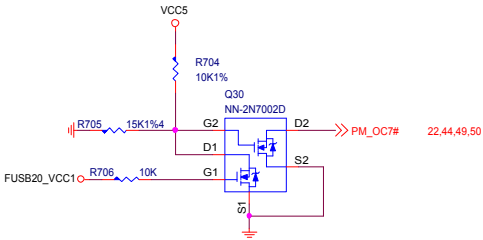
N31-2051BG1-H06



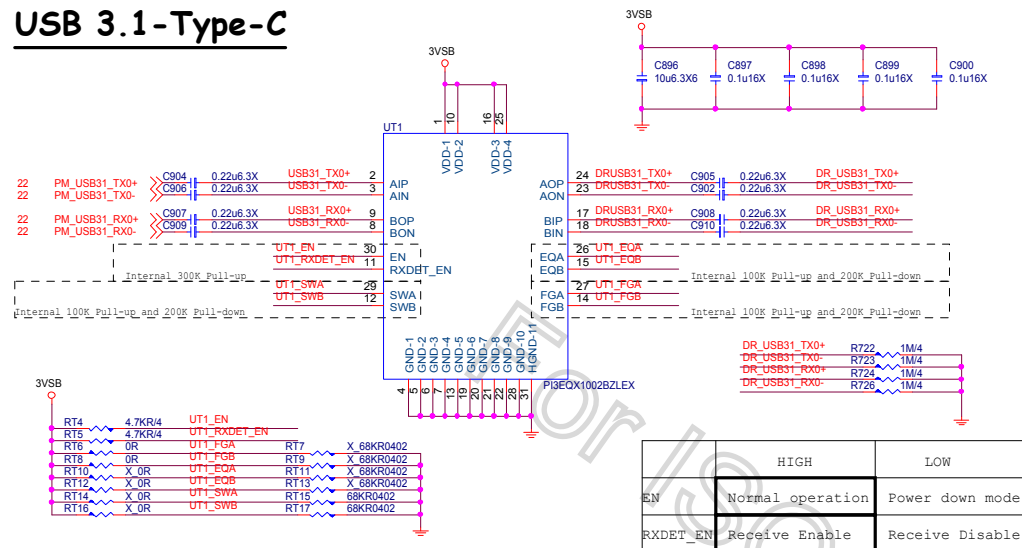
Main:D0G-05A0529-A68  
AVL:D0G-45B0510-I14



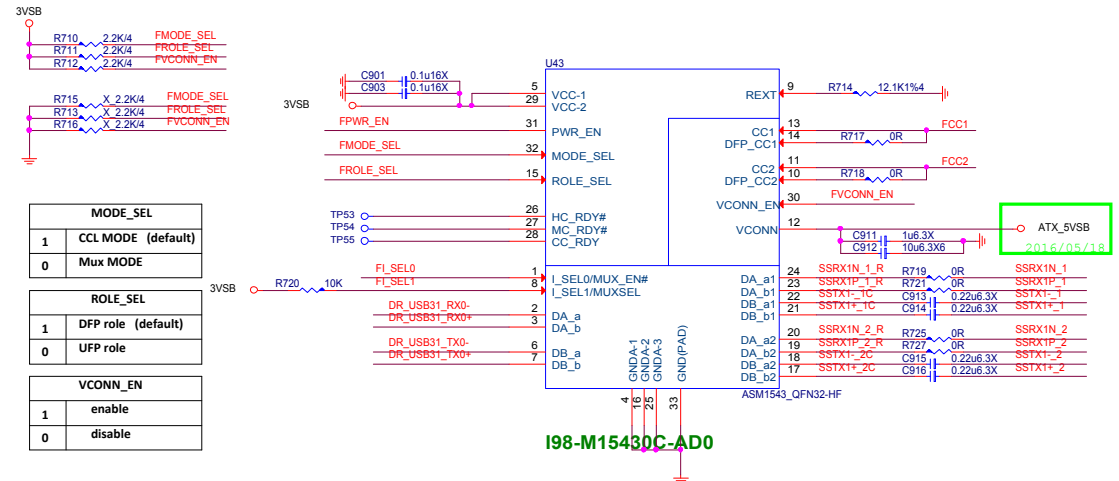
N31-2051BG1-H06



# USB 3.1-Type-C



# USB Type-C MUX with Configuration Channel (CC)



EQA/B are the selection pins for the equalization selection

EQA/B	Equalizer setting (dB)
0	5.1
R	1.9
F	3.5
1	6.8

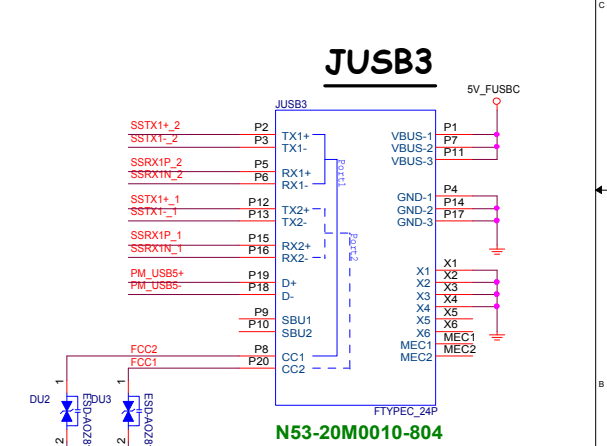
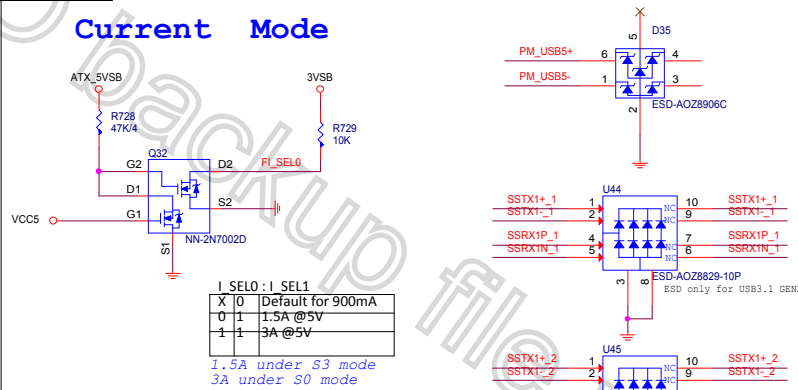
Flat Gain Setting:  
FGA/B are the selection bits for the DC gain

FGA/B	dB
0	-3
R	-1.5
F	0 (Default)
1	+2

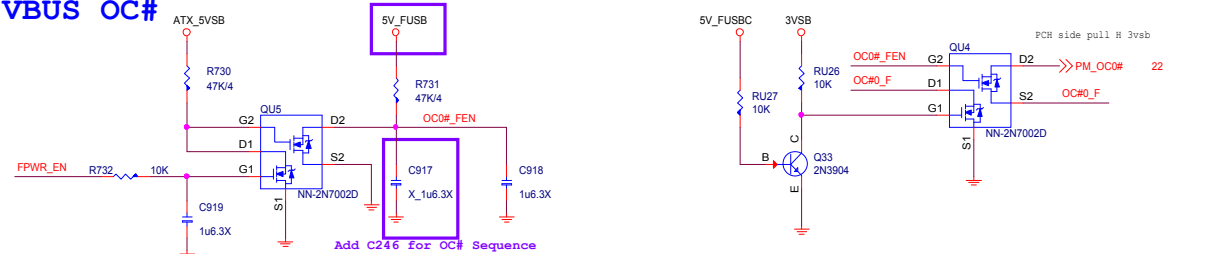
-1dB compression point linear Swing Setting:  
SWA/B are the selection bits for the output linear swing setting

SWA/B	mVppd
0	800
R	1200
F	1000 (Default)
1	1100

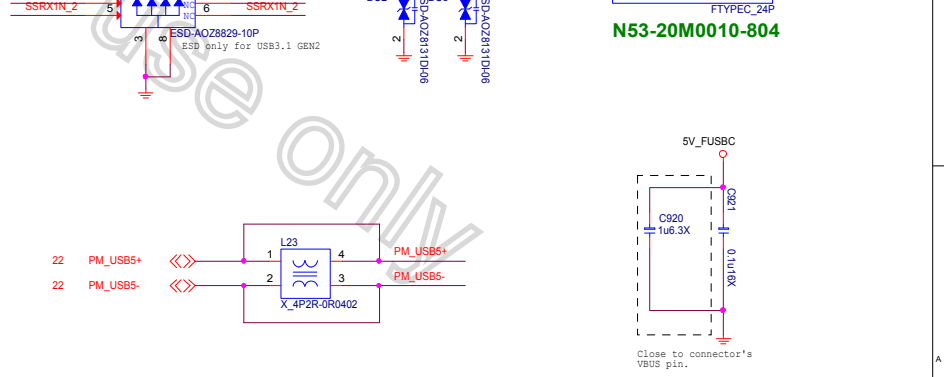
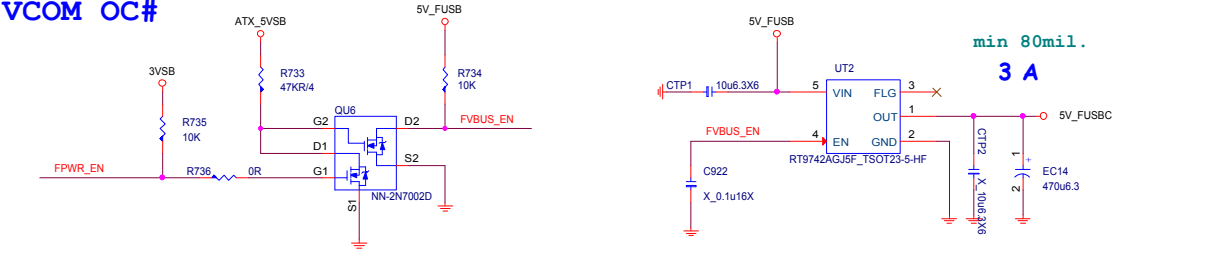
## Current Mode



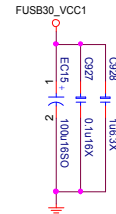
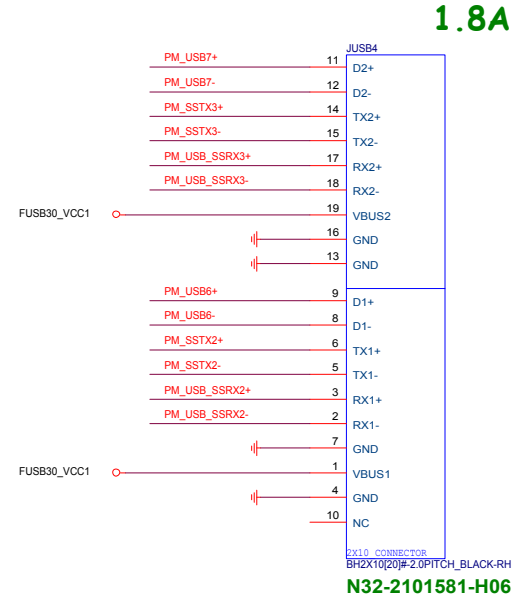
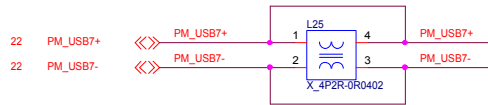
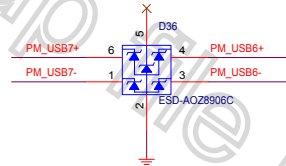
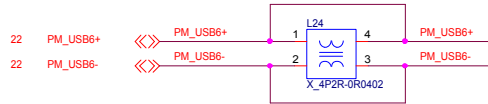
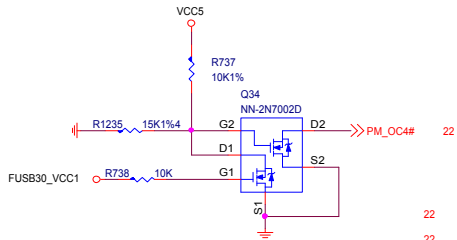
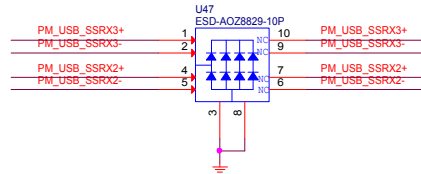
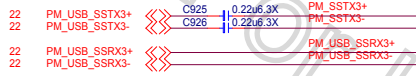
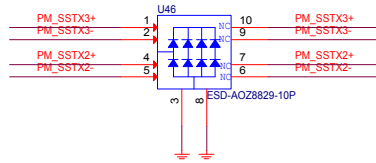
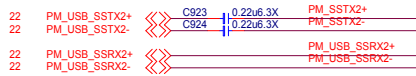
## VBUS OC#



## VCOM OC#

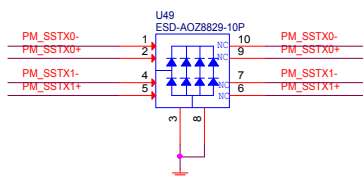
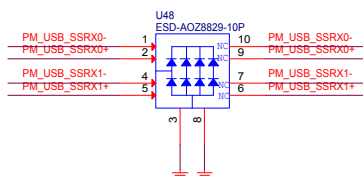


USB 3.0-JUSB4



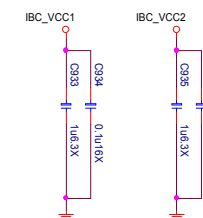
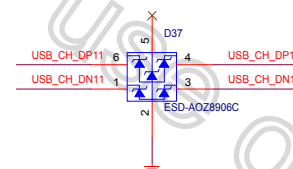
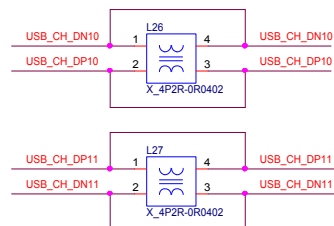
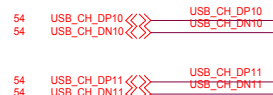
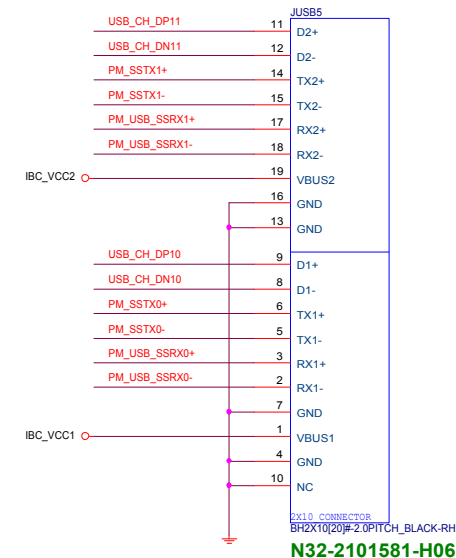
# USB 3.0-JUSB5 With Charge(BC1.2)

1.7A+1.7A

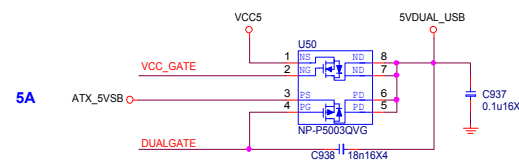
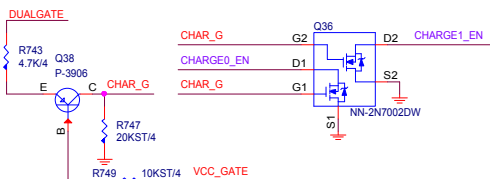
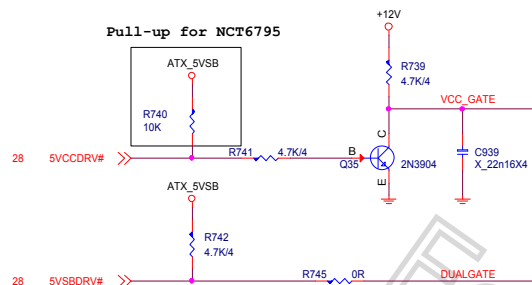


USB3.0  
D0G-06A050C-A68 Main  
D0G-05A0300-I14 AVL

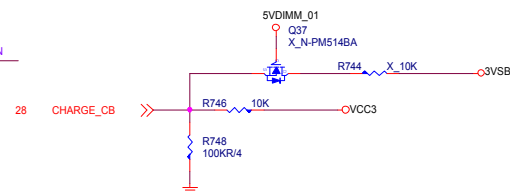
USB2.0  
D0G-0200529-A68 Main  
D0G-0100619-I05 AVL



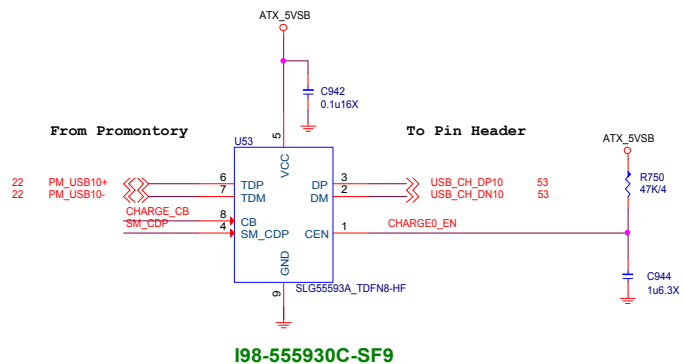
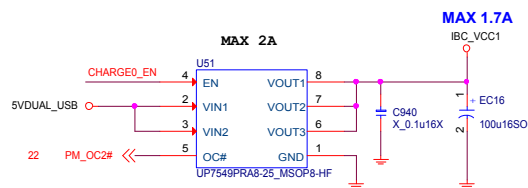
## 5VDUAL\_USB



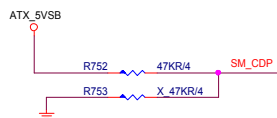
Pin power : I\_3VSB  
Register power : I\_3VSB  
Register reset : I\_3VSB



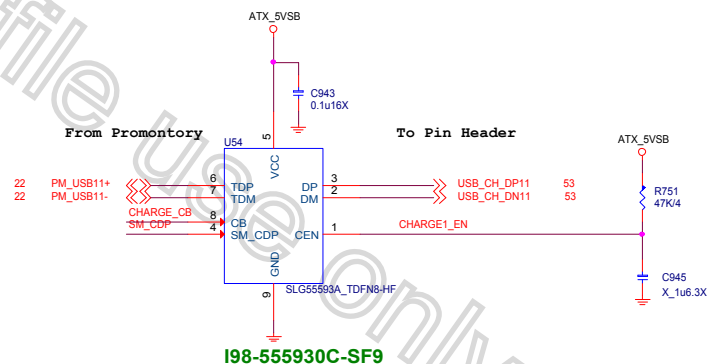
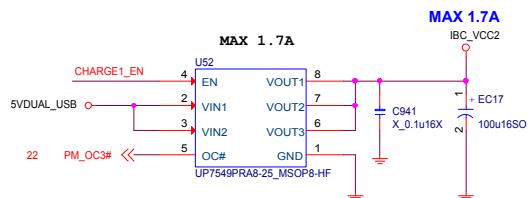
## USB POWER PORT 0 For USB Charging



I98-555930C-SF9

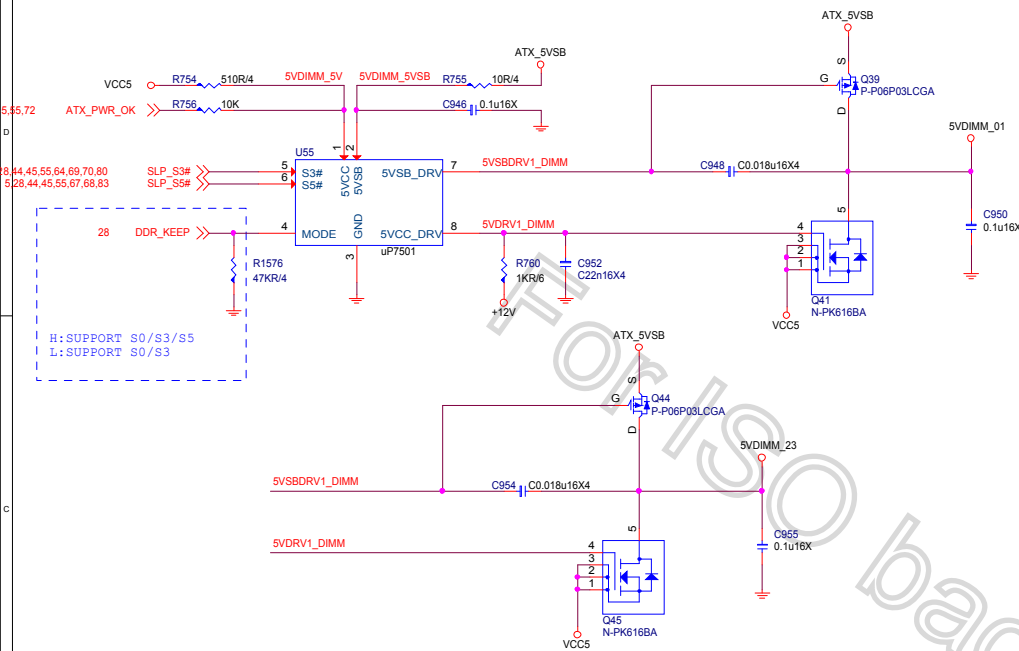


## USB POWER PORT 1 For USB Charging

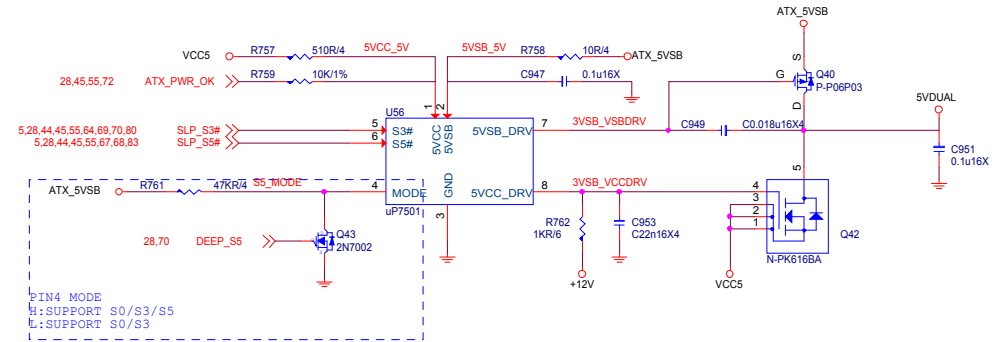


I98-555930C-SF9

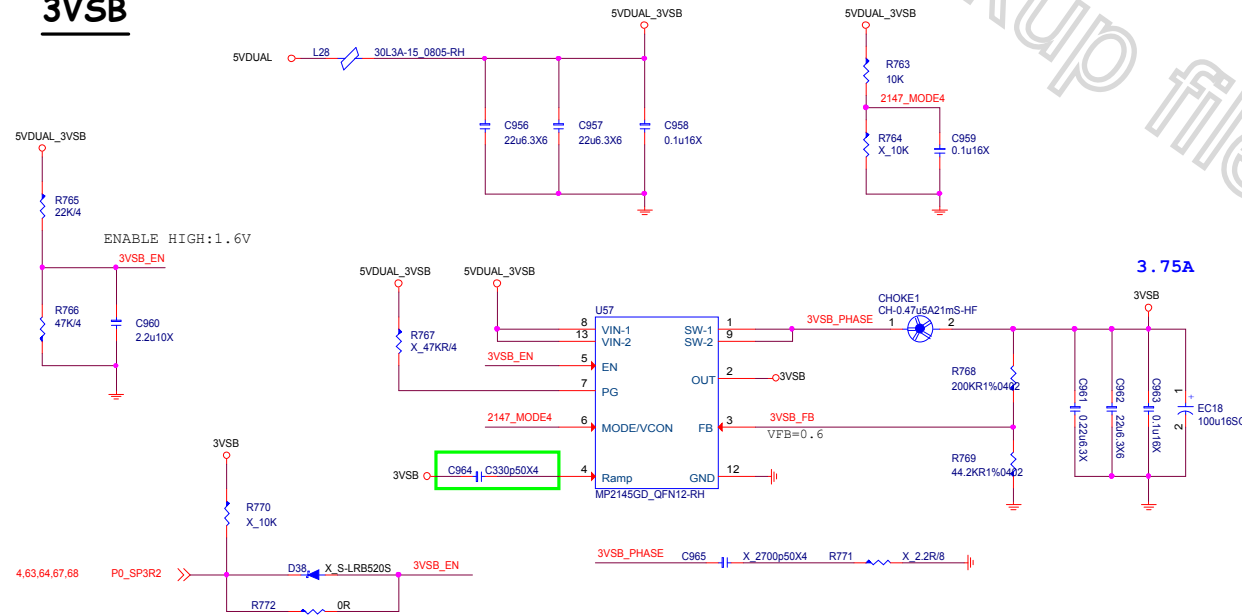
# 5VDIMM FOR DDR



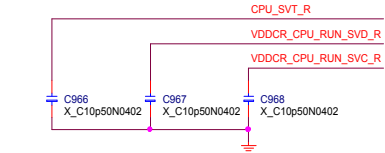
# 5VDUAL For 3VSB、CPU 1.8V、VDDP



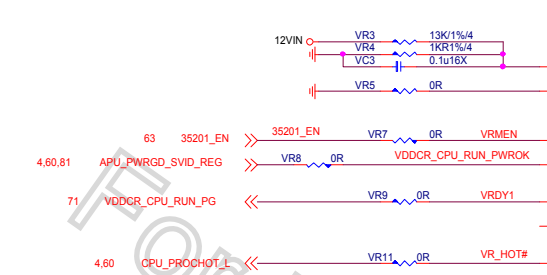
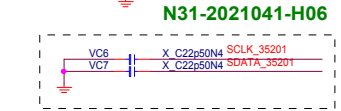
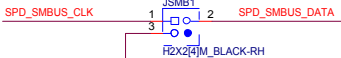
# 3VSB



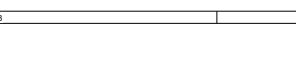
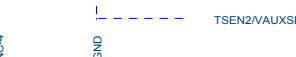
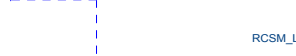
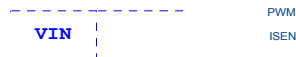
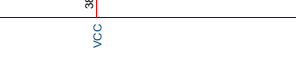
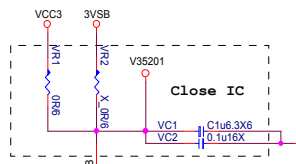
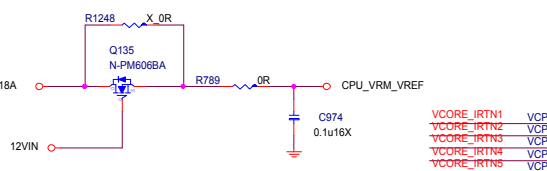
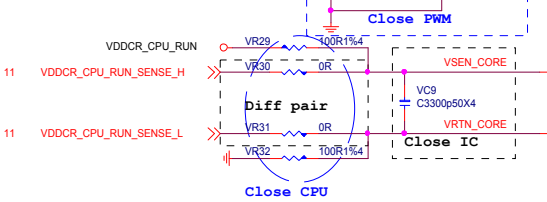
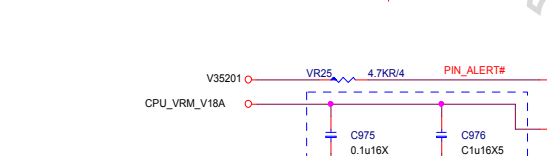
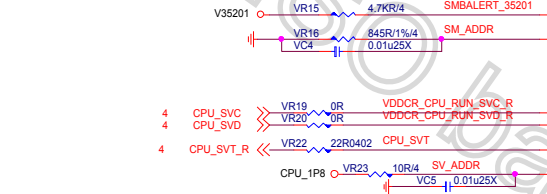
BOOT VOLTAGE		Pre_PWROK Metal VID
SVC	SVD	
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



5,15,17,36,44,60,67,68,73,74,75,79,80  
5,15,17,36,44,60,67,68,73,74,75,79,80

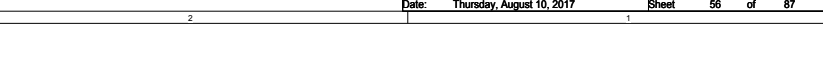
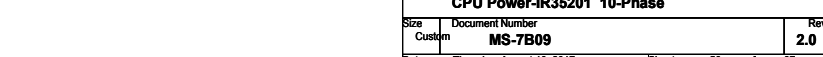
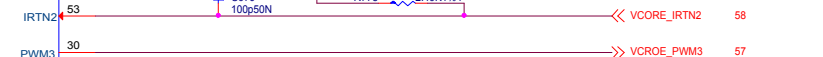
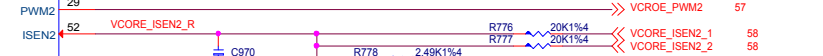
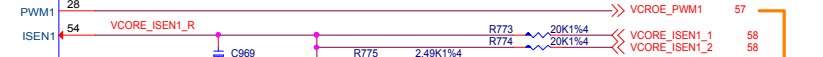


Condition as TSEN point

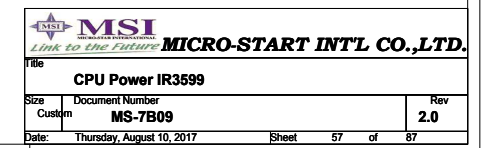


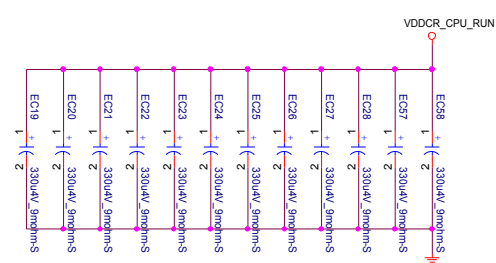
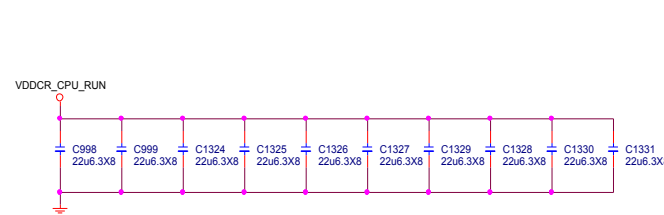
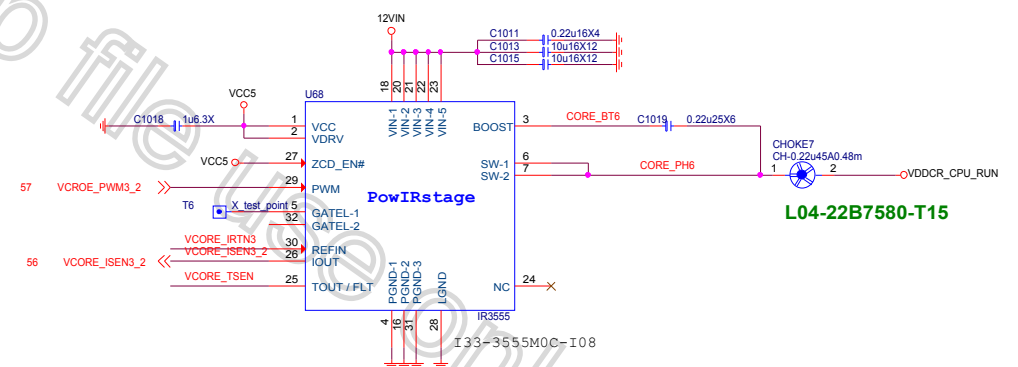
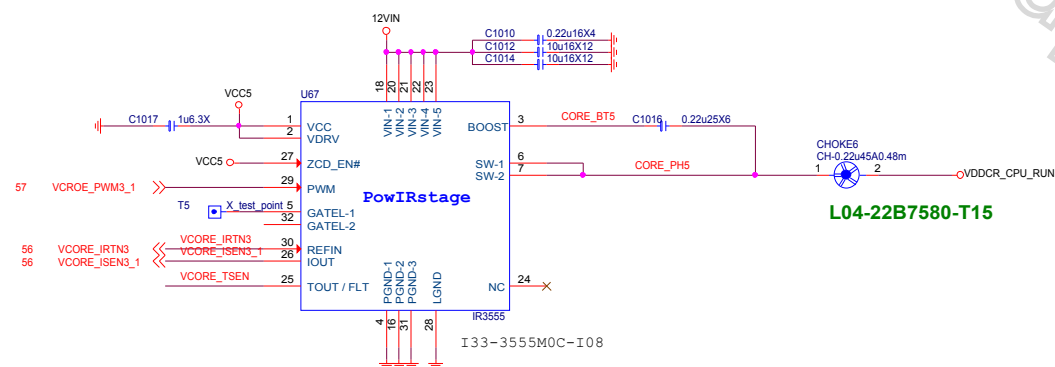
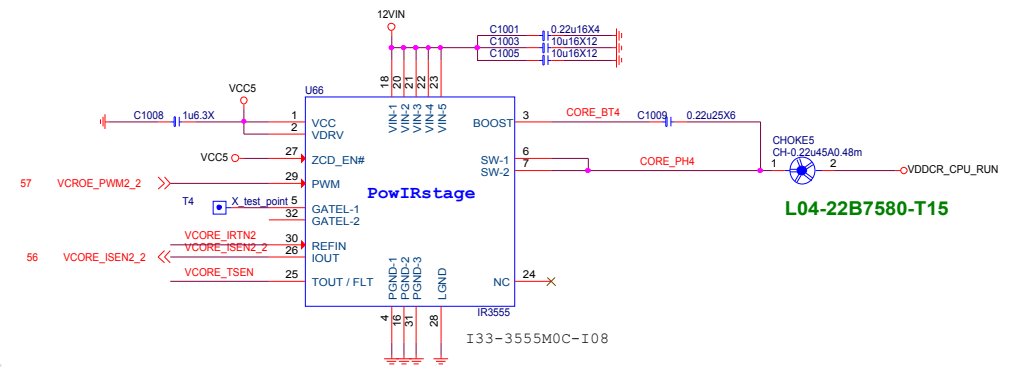
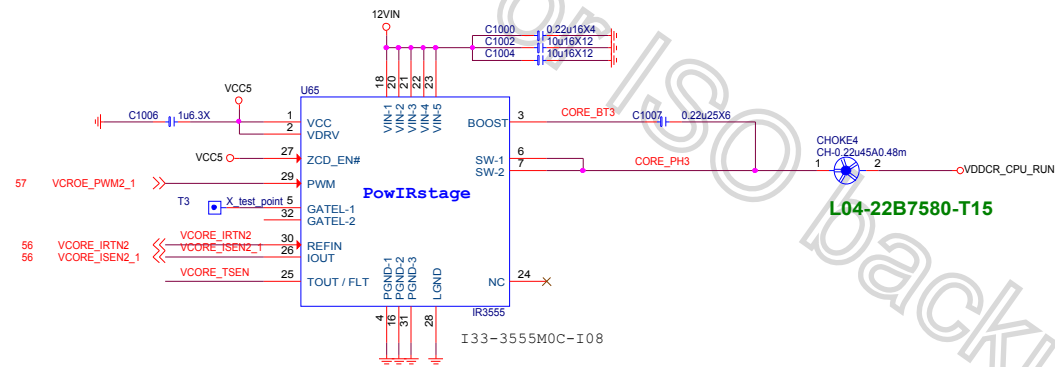
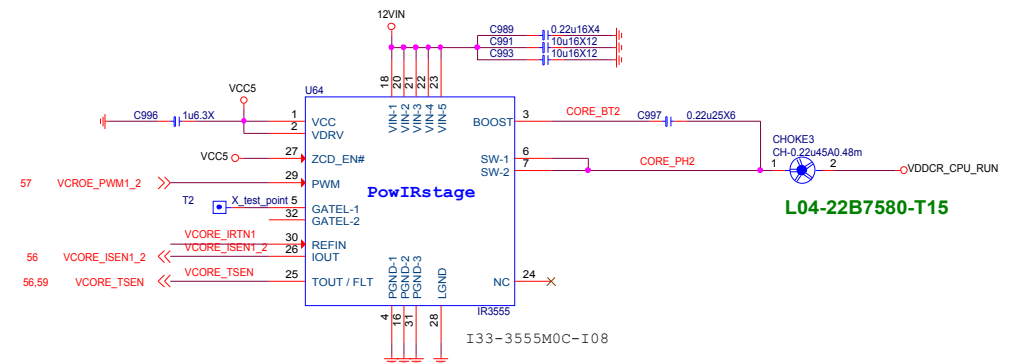
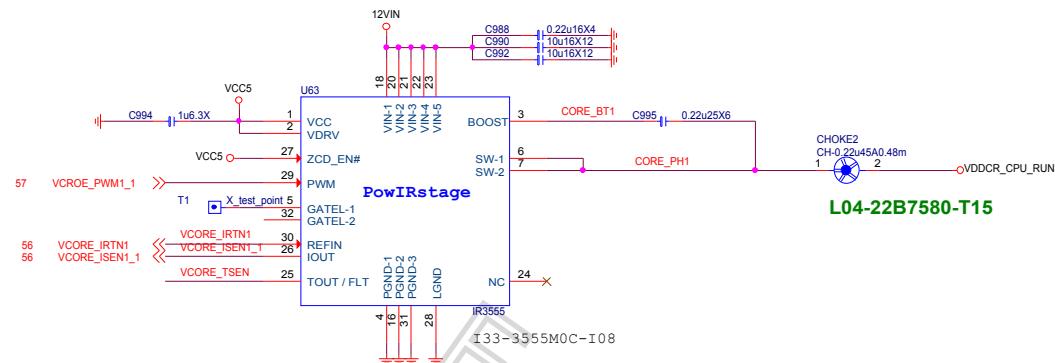
Vcore: ICC Max 240A  
LL: 0.3 mohm  
OCP: 400A

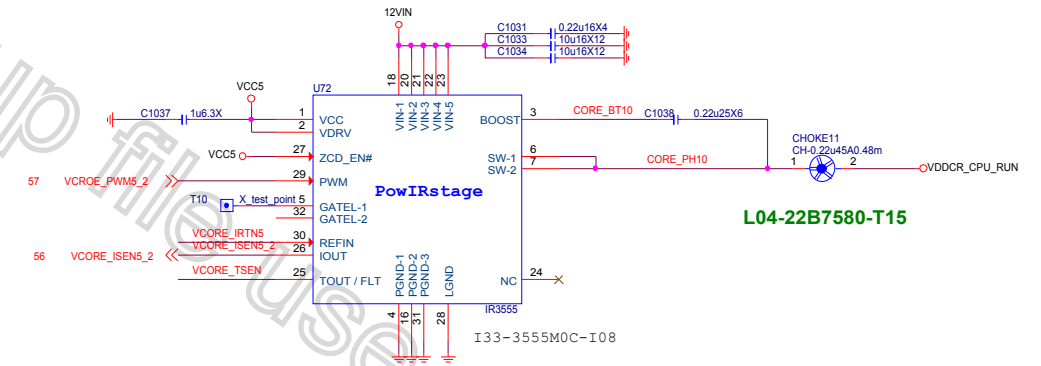
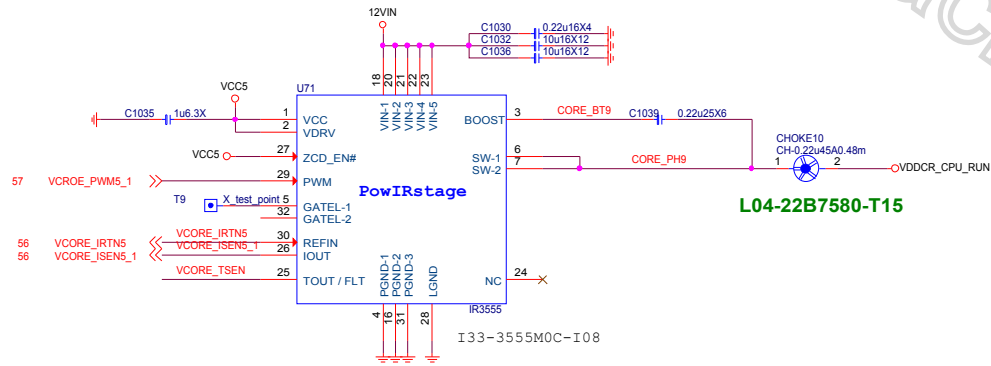
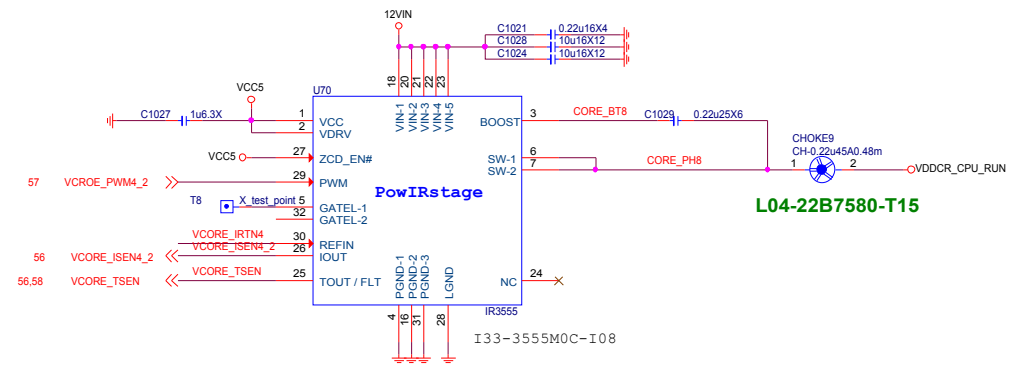
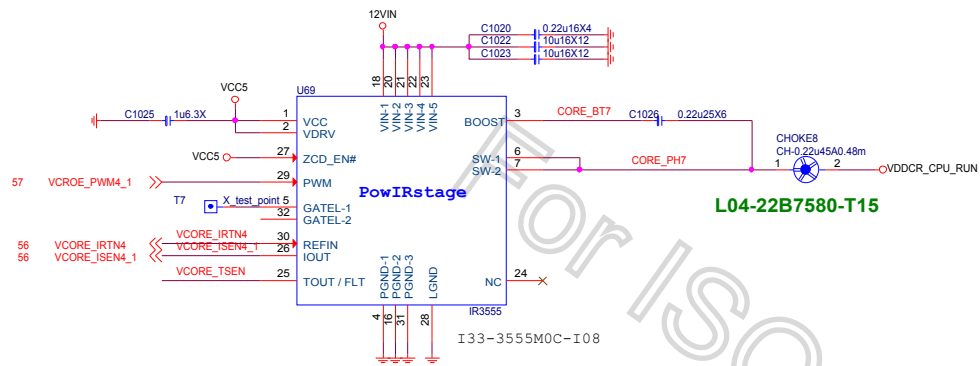
Phase 1 close to CPU power pin.



## VCORE Double 10-PHASE

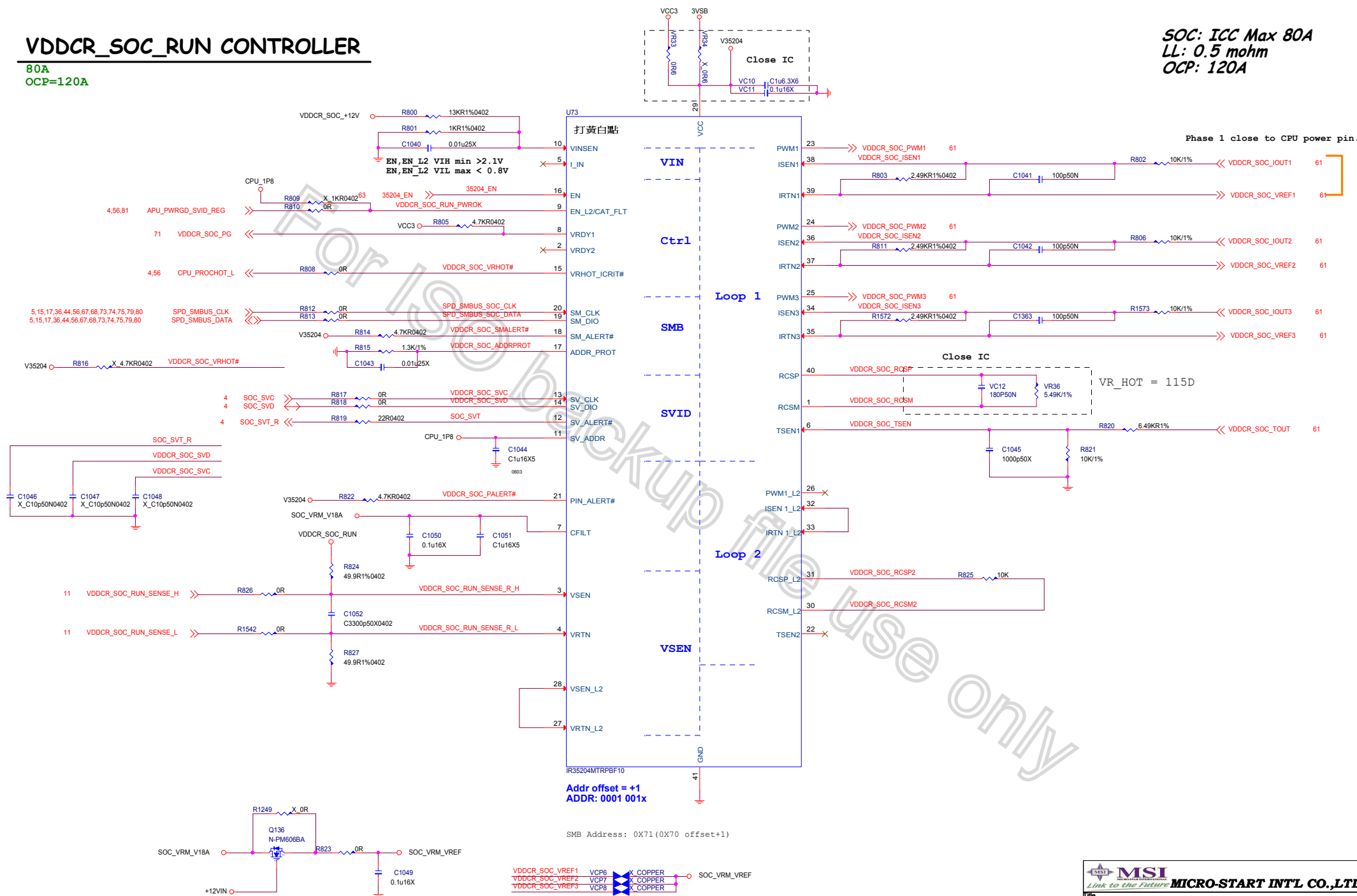




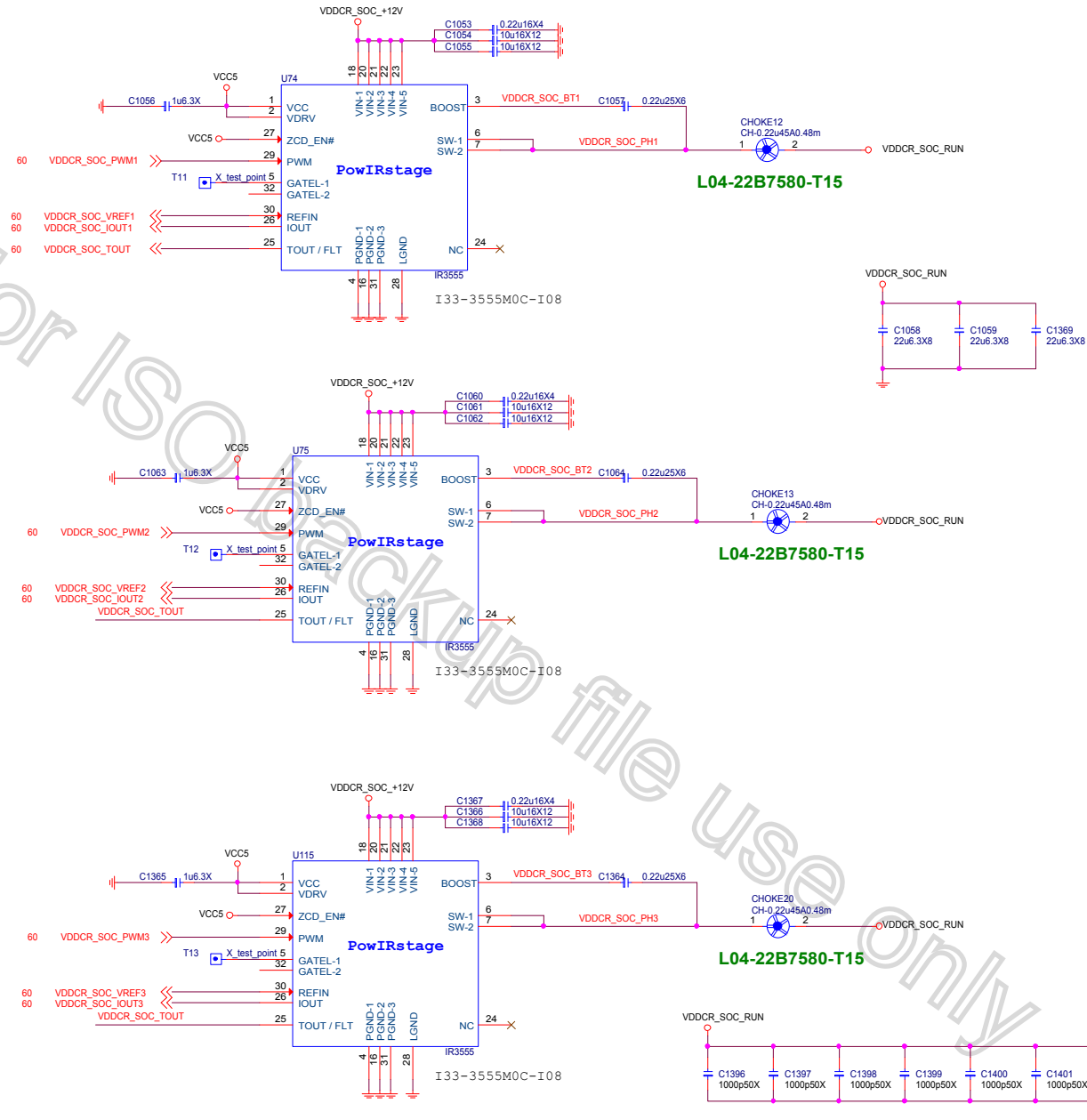


80A  
OCP=120A

SOC: ICC Max 80A  
LL: 0.5 mohm  
OCP: 120A

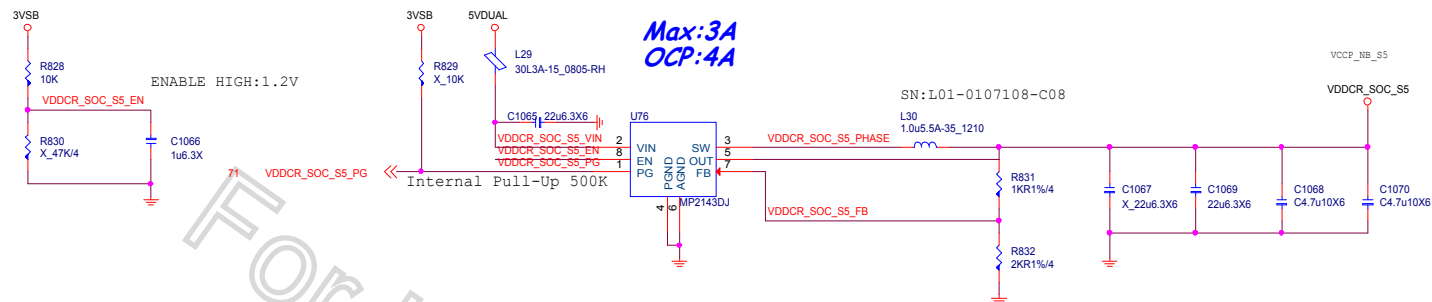


## 3-PHASE

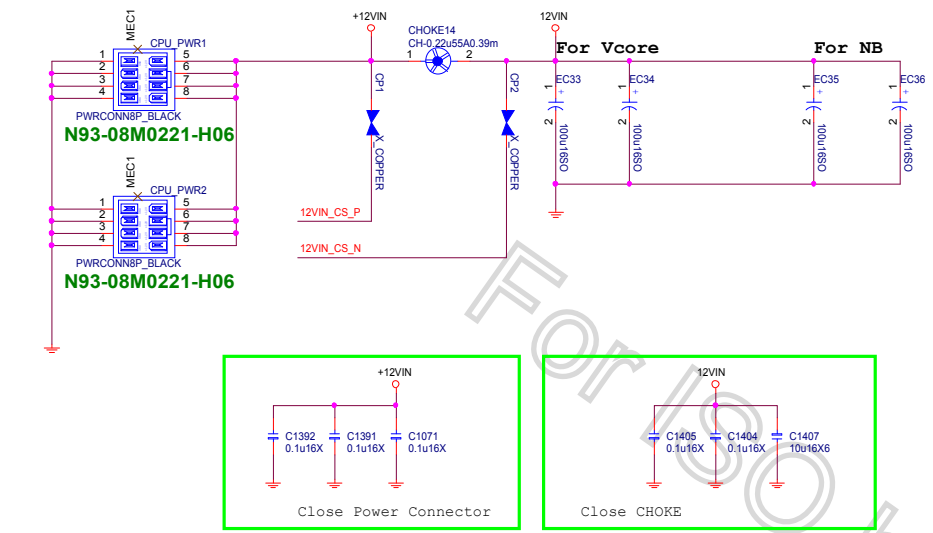


# VDDCR\_SOC\_S5 0.9V

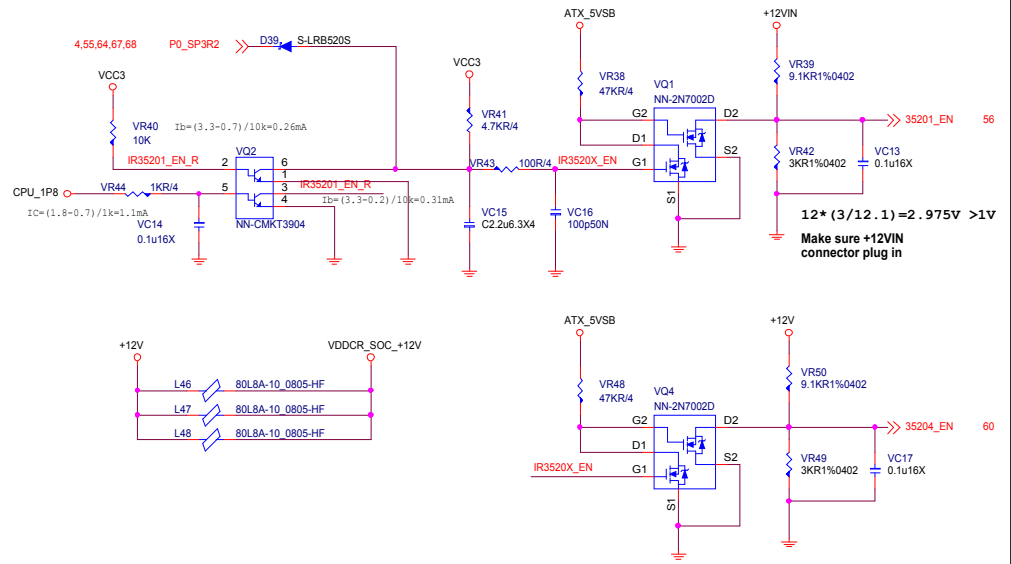
2A



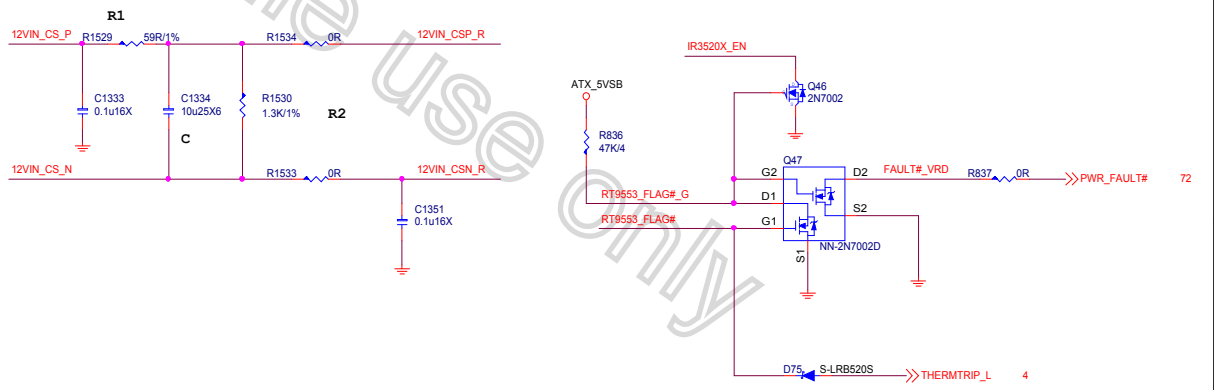
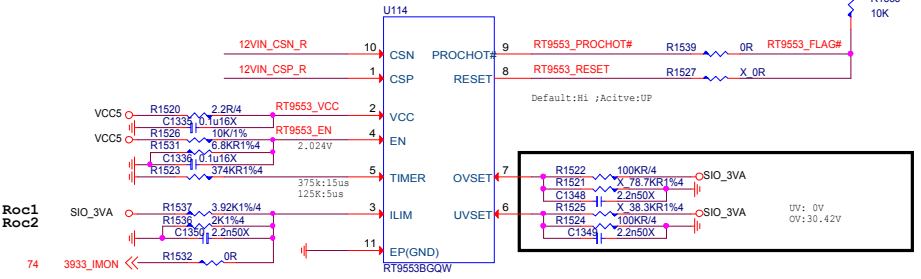
CPU POWER CONNECTOR



VRM\_Enable circuit

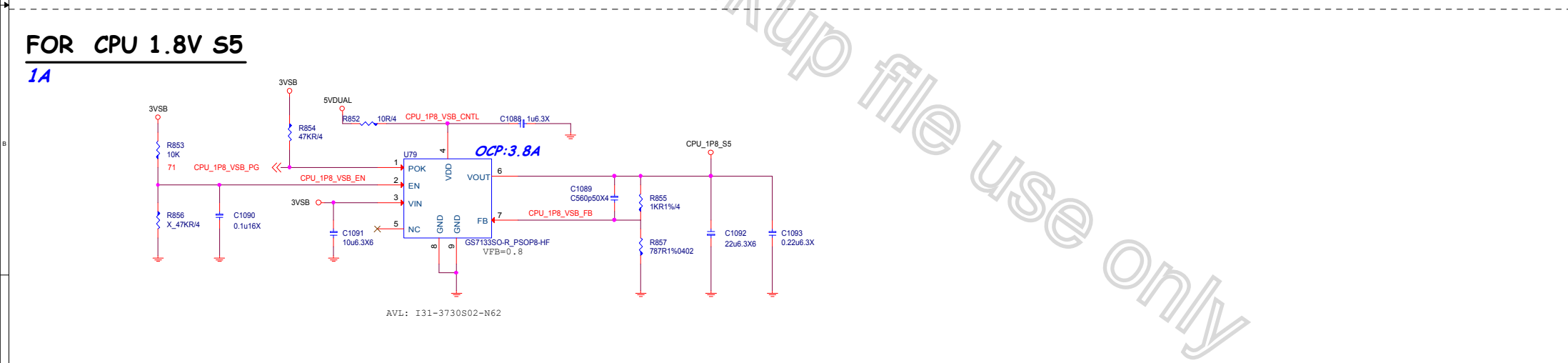


RT9553 CURRENT SENSE

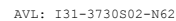


$I_{3933\_imon} * [R_{17} * R_{18} / (R_{17} + R_{18})] = I_{step} * R_{dcr} * 100$   
 $I_{3933\_imon} = 10\mu A / step$   
 $I_{step} = 4.785A$

## 3A

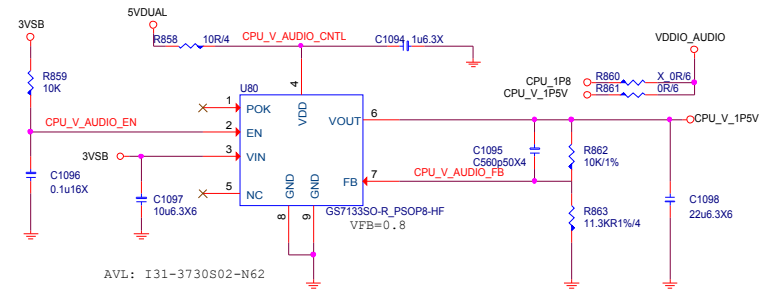


**1A**

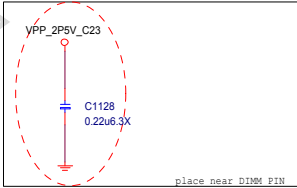
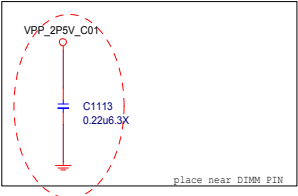


# VDDIO\_AUDIO Circuit

1.5V  
0.25A



2.5+0.25/-0.125V  
JE79 DDR4 max 3V

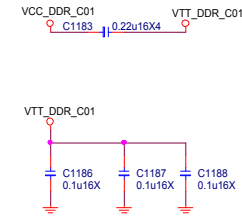
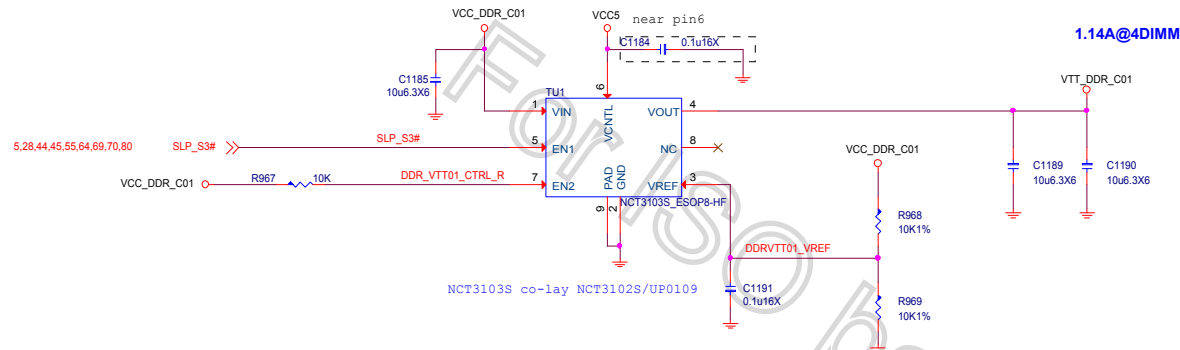






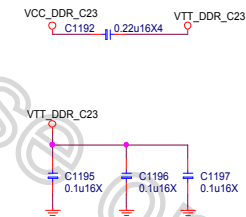
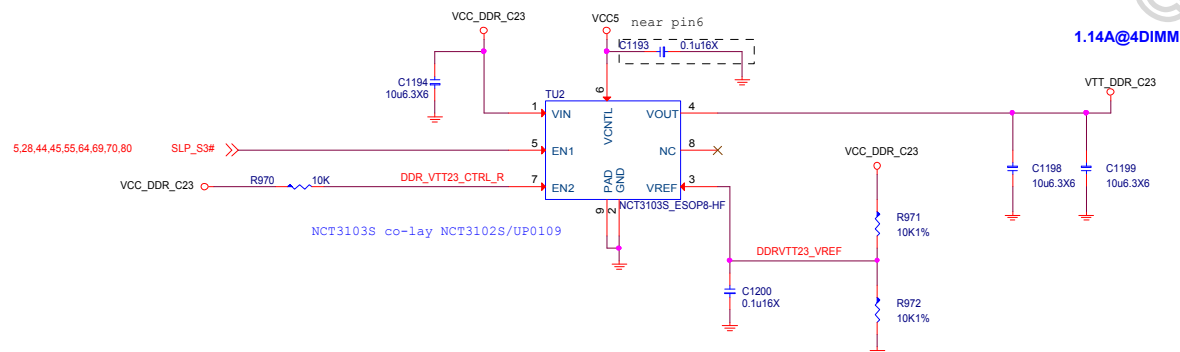
### DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



### DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



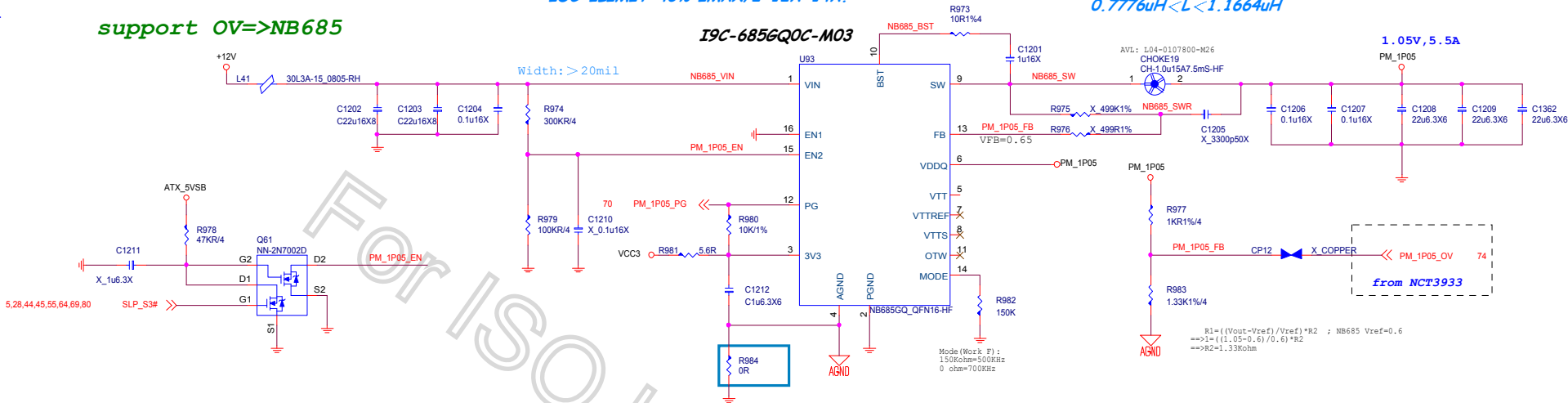
FOR Promontory 1.05V\_S0

1.05V  
S0:5.5A  
S5:0.05A

support OV=>NB685

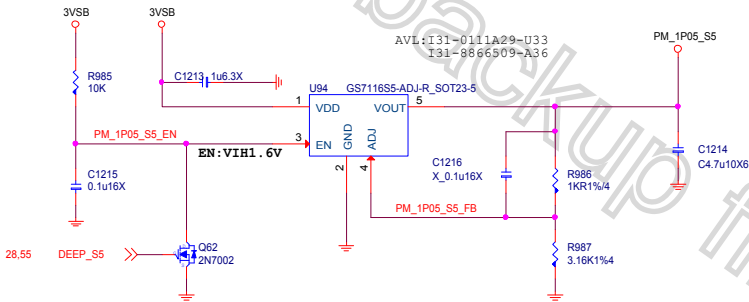
IMAX 10A  
ILIMIT=10A~12A  
IOC=ILIMIT+40%\*IMAX/2=12A~14A.

0.7776uH<L<1.1664uH



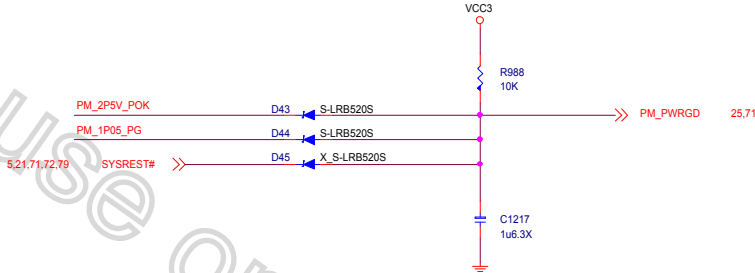
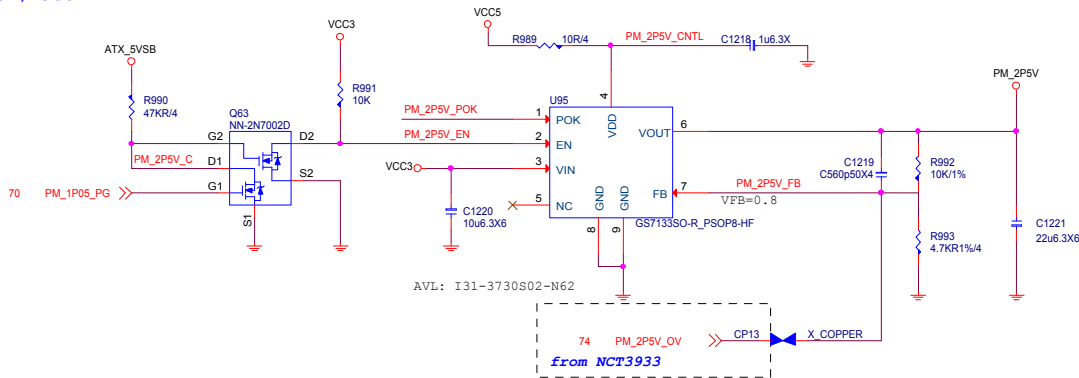
FOR Promontory 1.05V\_S5

0.05A

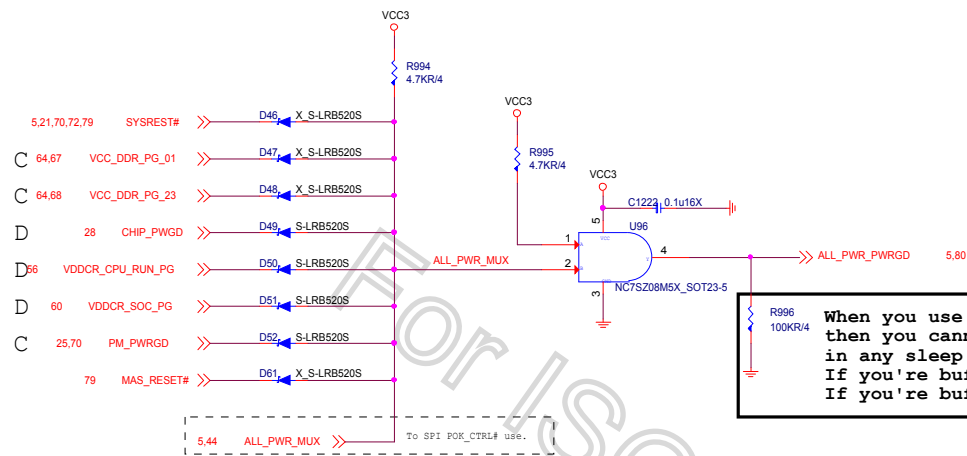


Promontory-2.5V

2.5V; 900mA

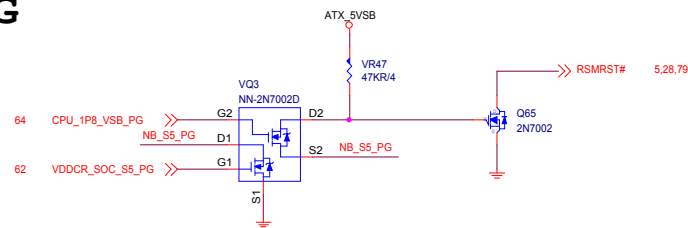


ALL POWER GOOD MUX

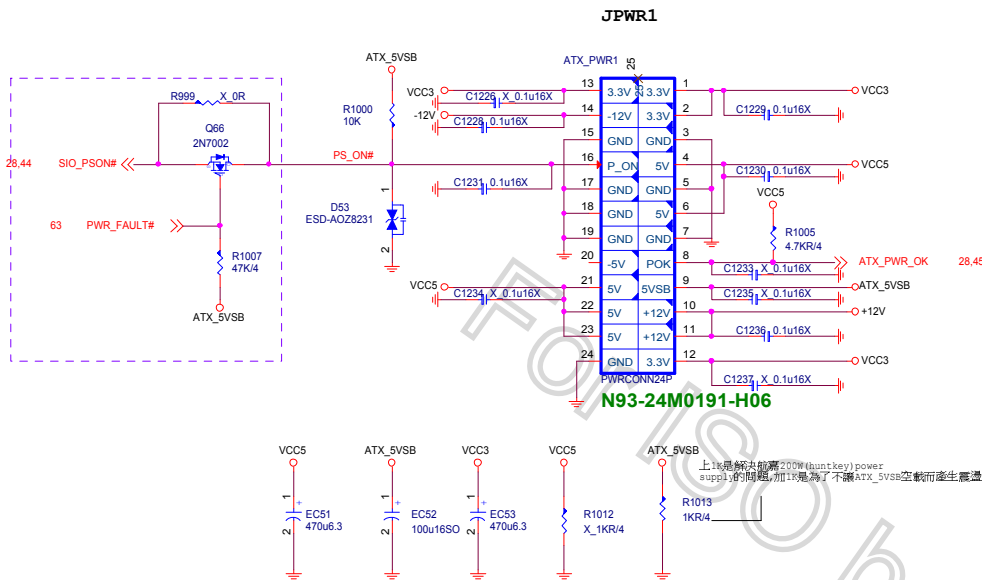


When you use external buffer  
then you cannot let APU PWR\_GOOD pin float  
in any sleep state.  
If you're buffer use 3.3V\_S0 and you need Pull-down 100K  
If you're buffer use 3.3V\_S5 and you don't need PD.

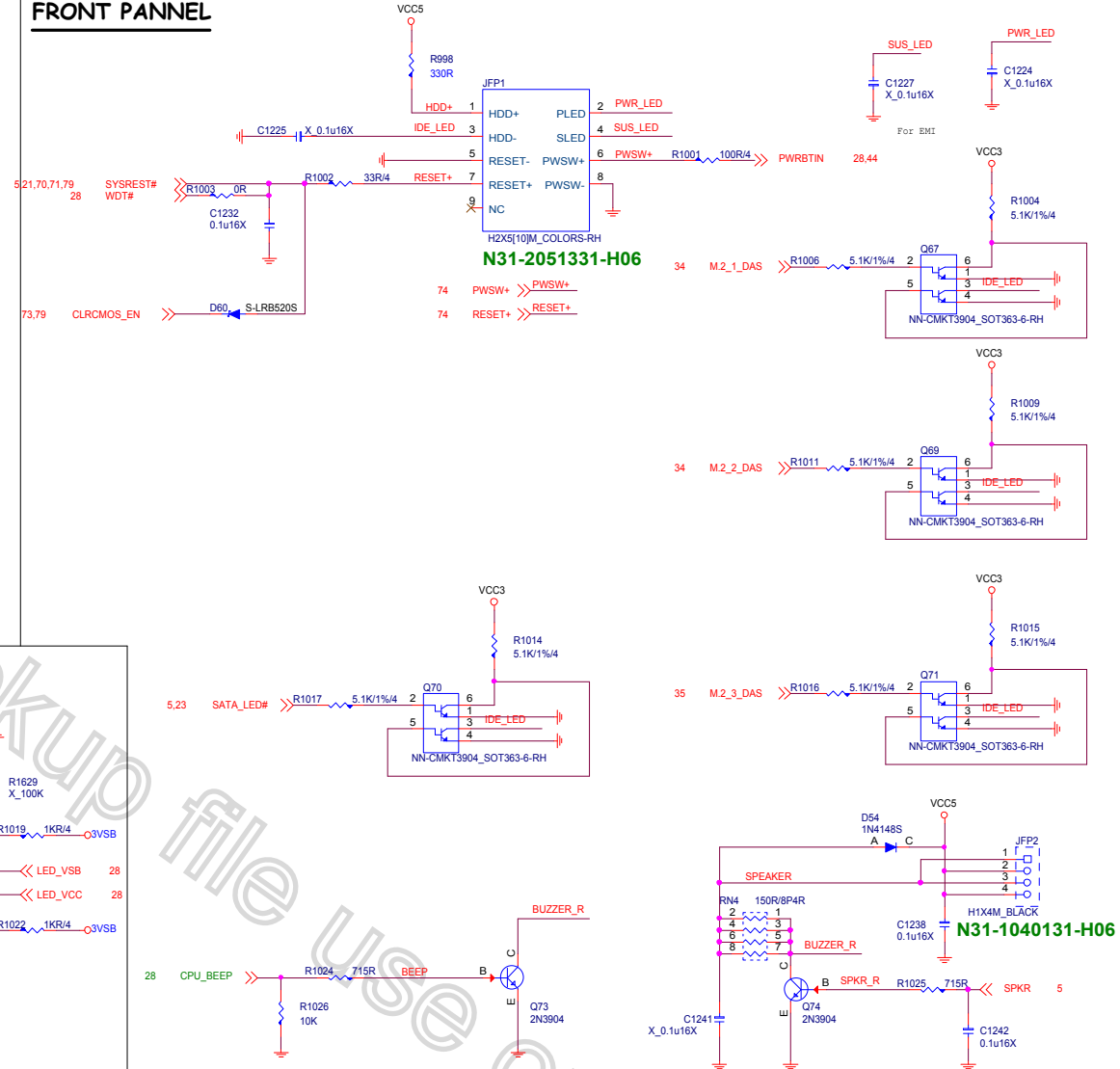
S0 PG  
S5 PG



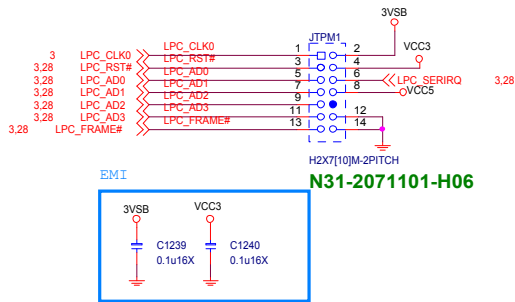
## ATX POWER CONNECTOR



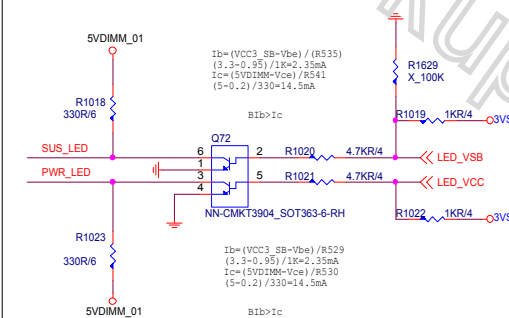
## FRONT PANNEL



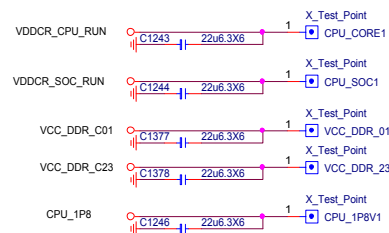
## TPM



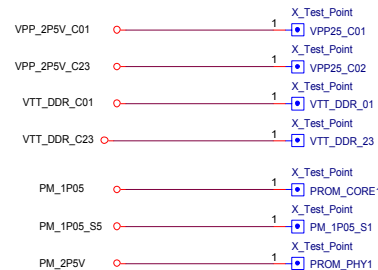
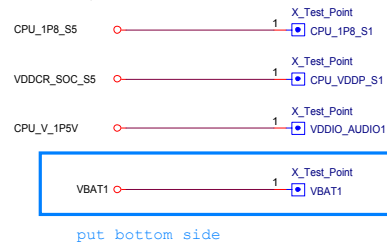
## LED ( for NCT6795D)



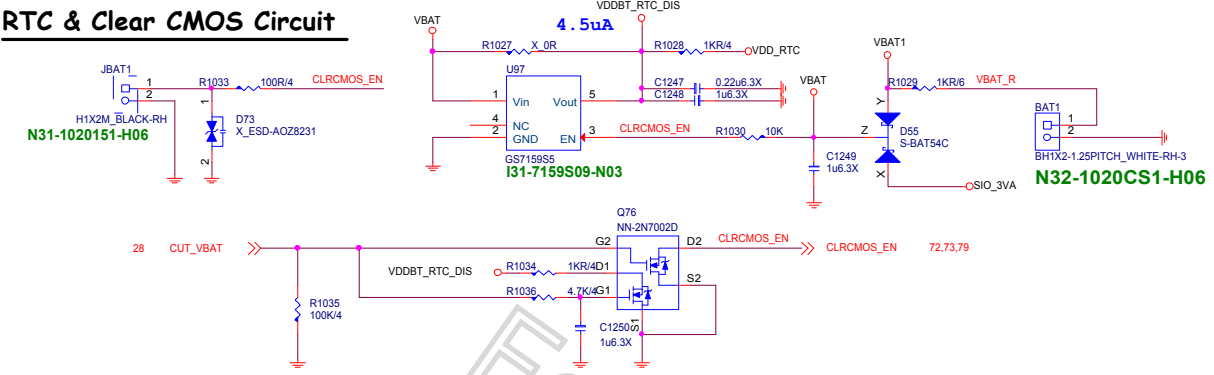
## Voltage Mearsure Point



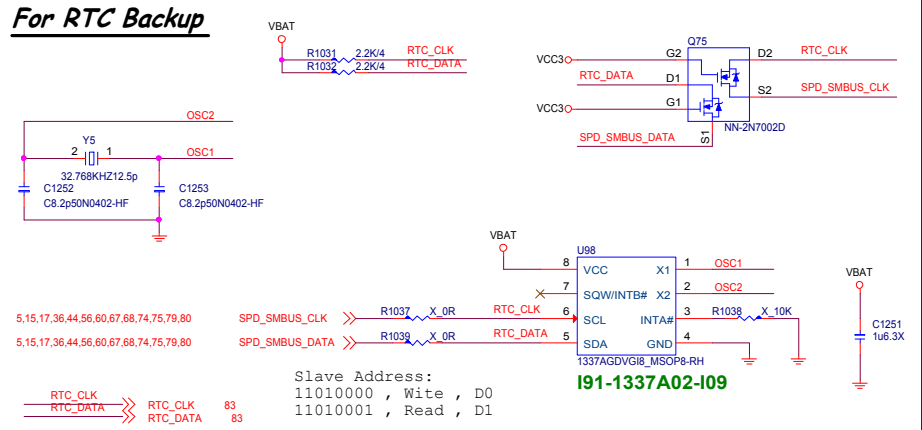
## Close to output of IC



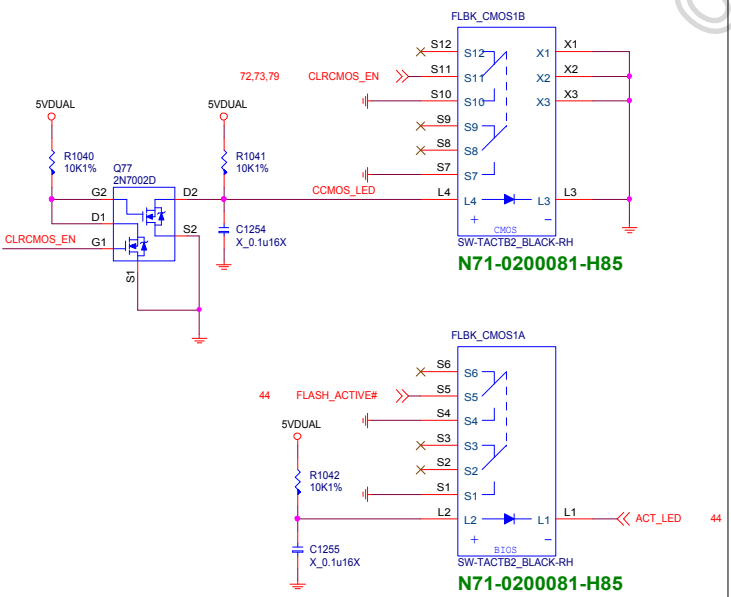
RTC & Clear CMOS Circuit



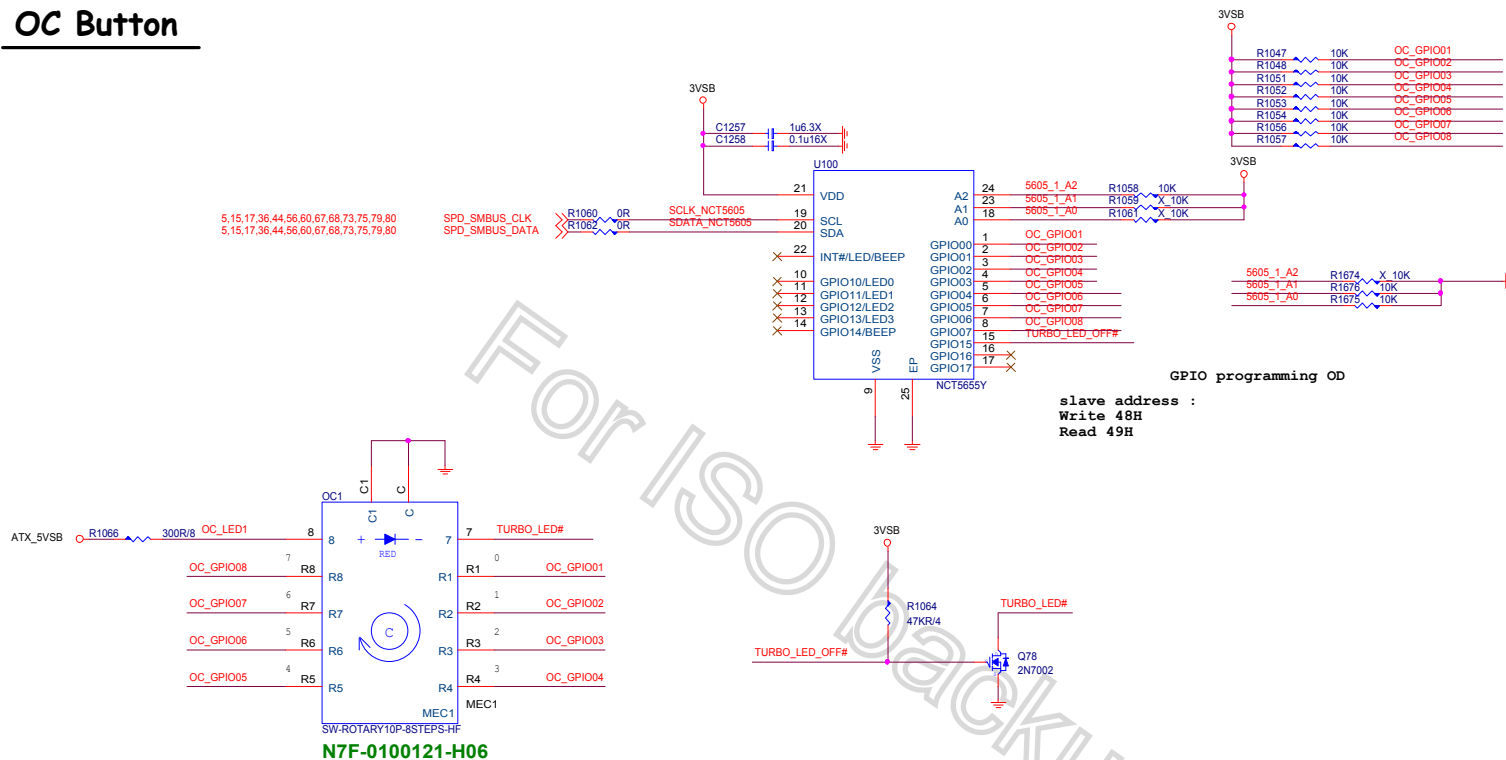
For RTC Backup



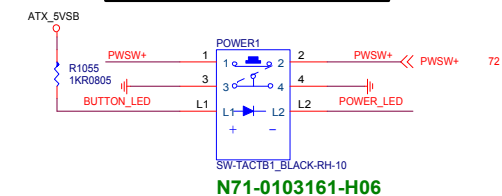
Clear CMOS&Flash Back button



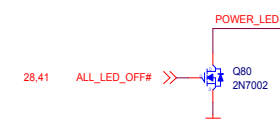
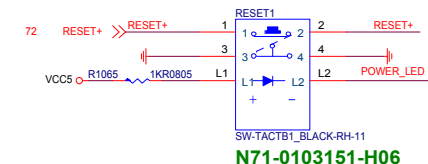
## OC Button



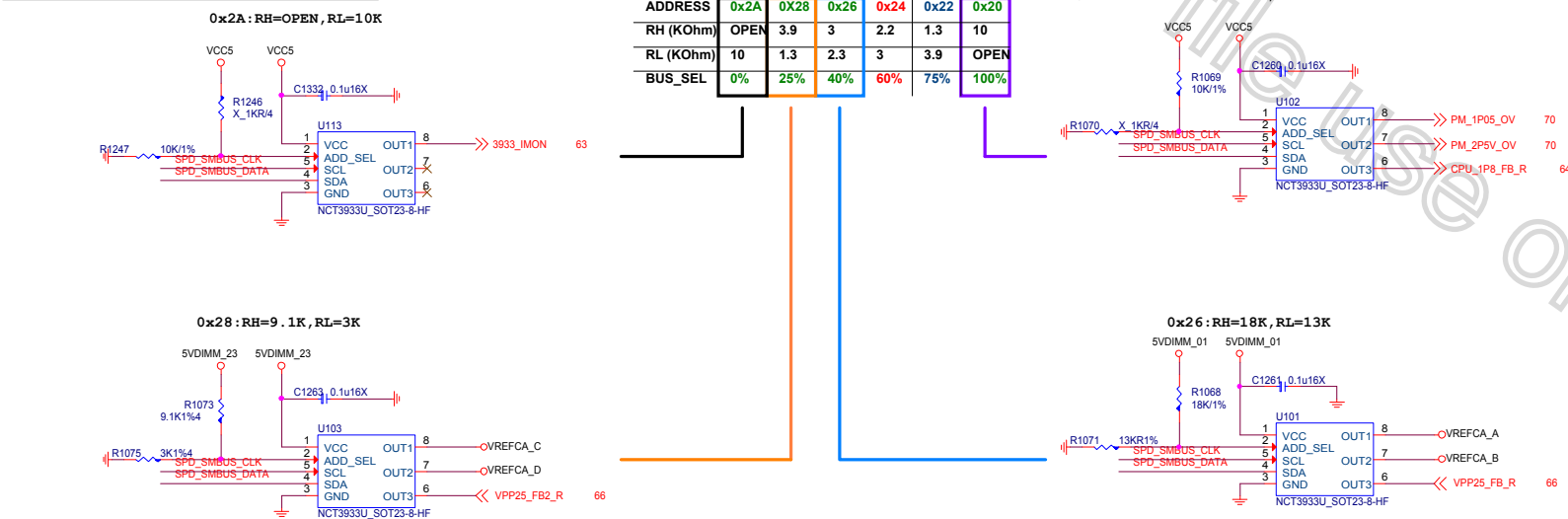
## Power ON Button



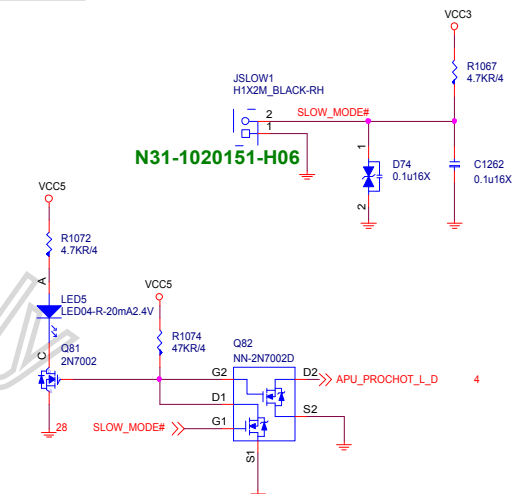
## Reset Button



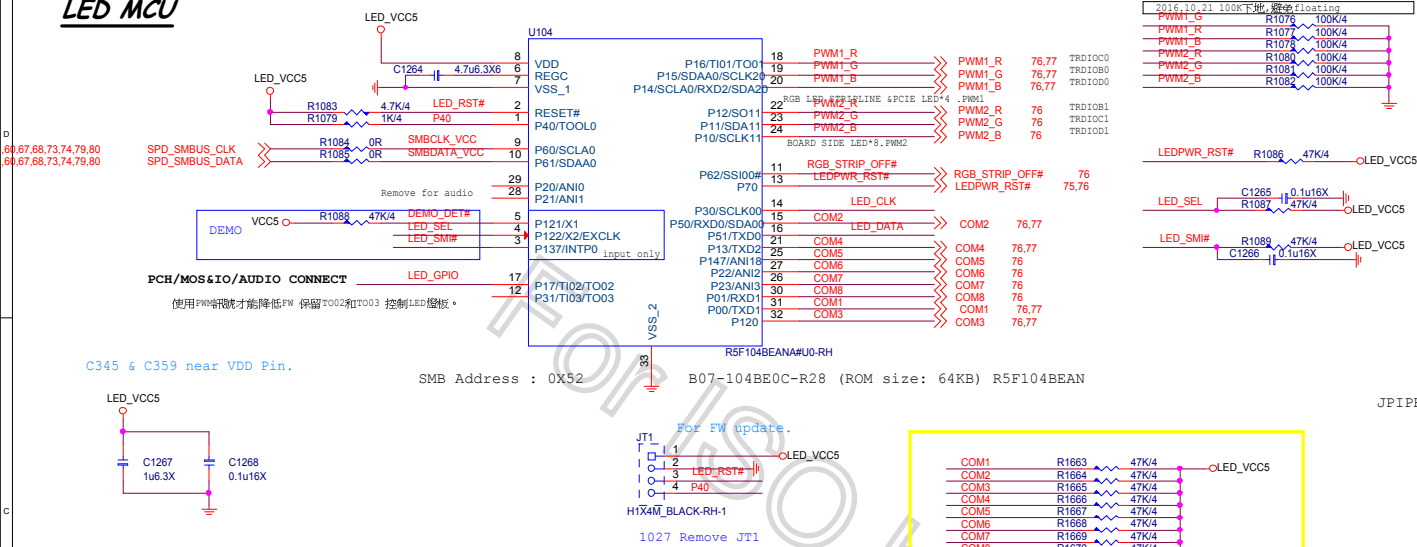
## Over Voltage Control IC



## Slow Mode



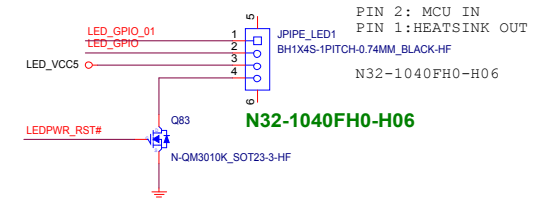
## LED MCU



Control	Net Name	PWM USE	Connector
PCH	LED_GPIO	No Use	JPIPE_LED1
AUDIO Cover	LED_GPIO_01	No Use	JPIPE_LED2
MOS/IO cover	LED_GPIO_02	No Use	JPIPE_LED3
LED STRIPLINE	RGB_STRIP_OFF#	PWM1	JLED1
Board Side LED	COM1-8	PWM2	RGB LED
PCIE Side LED	COM1-4	PWM1	RGB LED

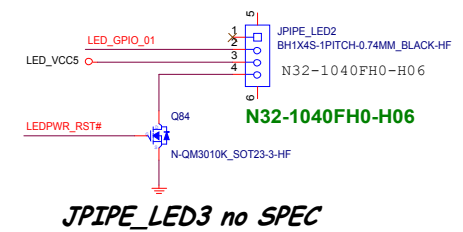
## 1 PCH HEATSINK LED

### PCS LED\*0.16W=W



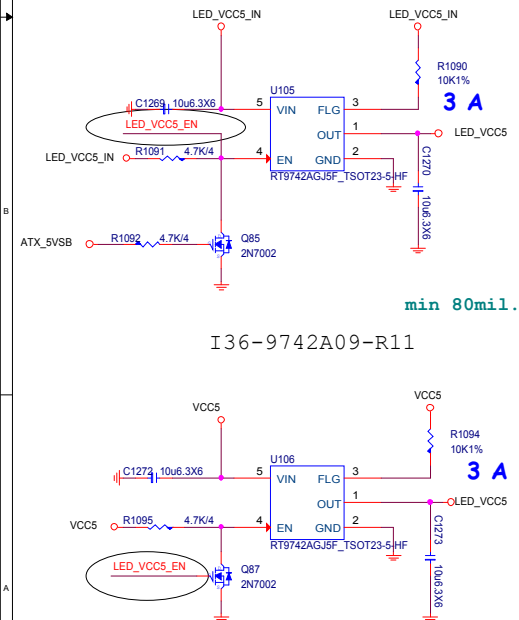
## 2 AUDIO/IO Cover LED

### PCS LED\*0.16W=W

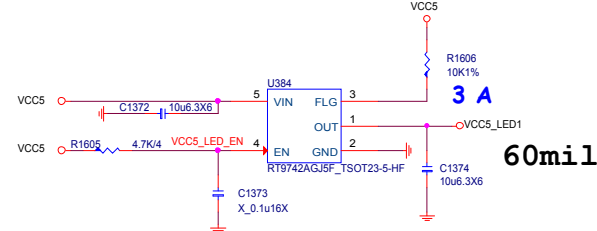
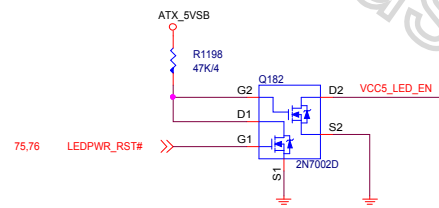
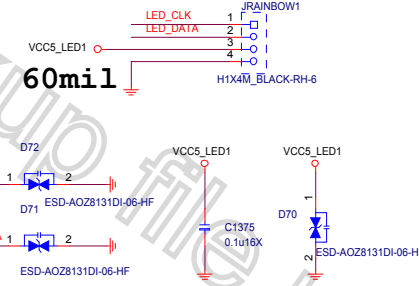
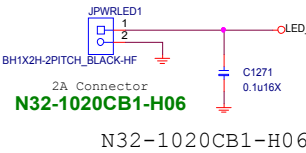
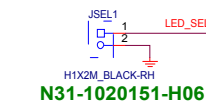
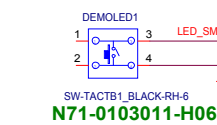


### JPIPE\_LED3 no SPEC

## EXTERNAL POWER INPUT

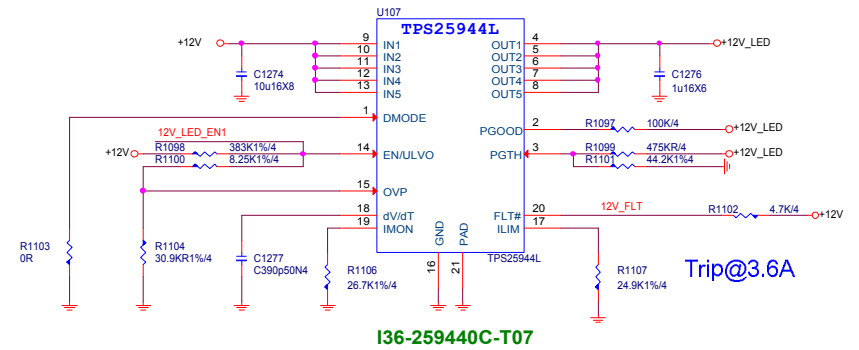
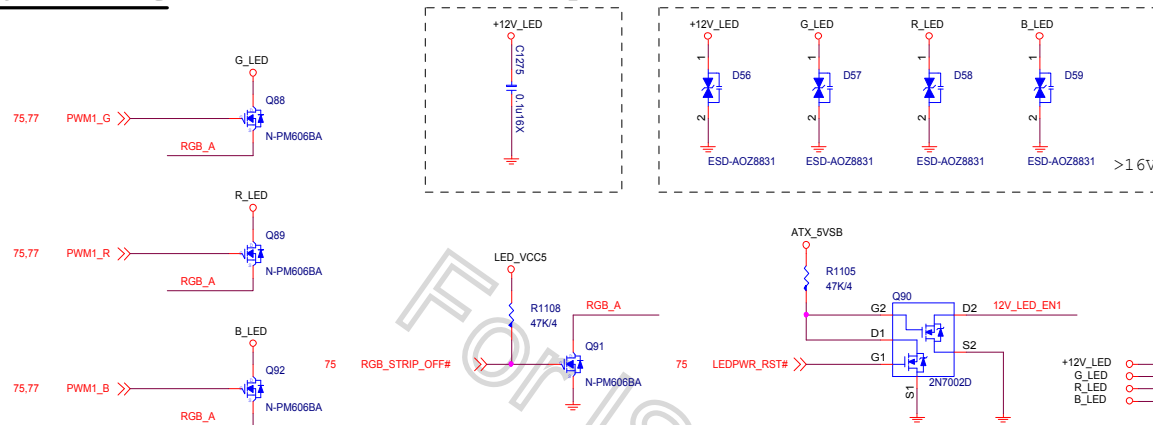


## LED Demo Button



## LED STRIPLINE

2016.07.06 only reserve now  
2016.08.02 Add +12V\_LED 0.1uF 2016.08.02 stuff ESD



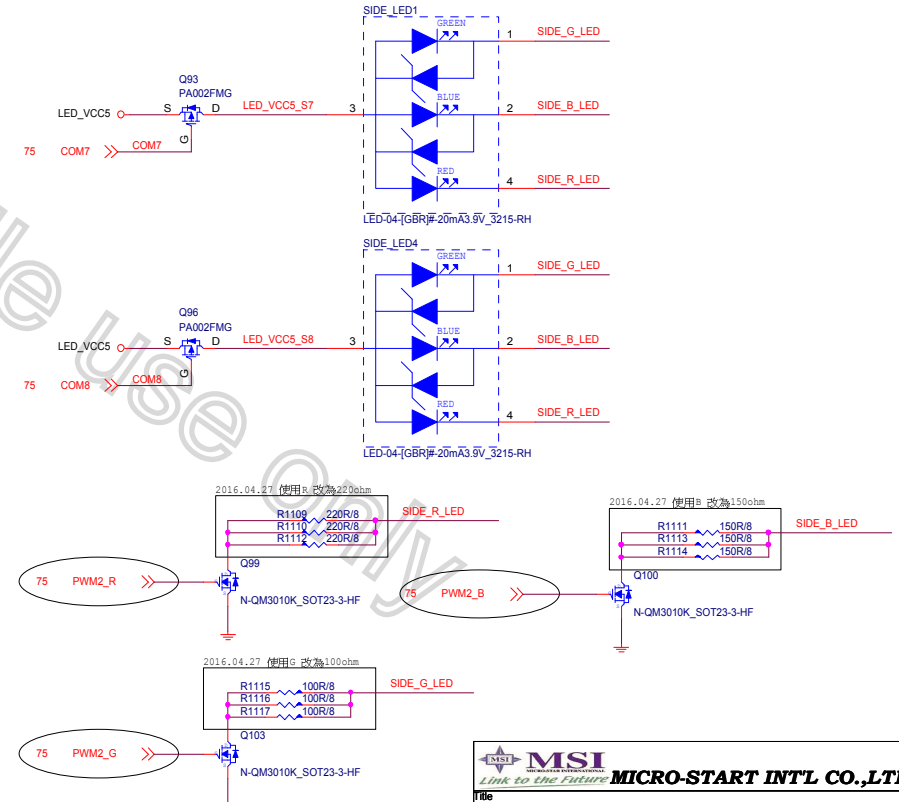
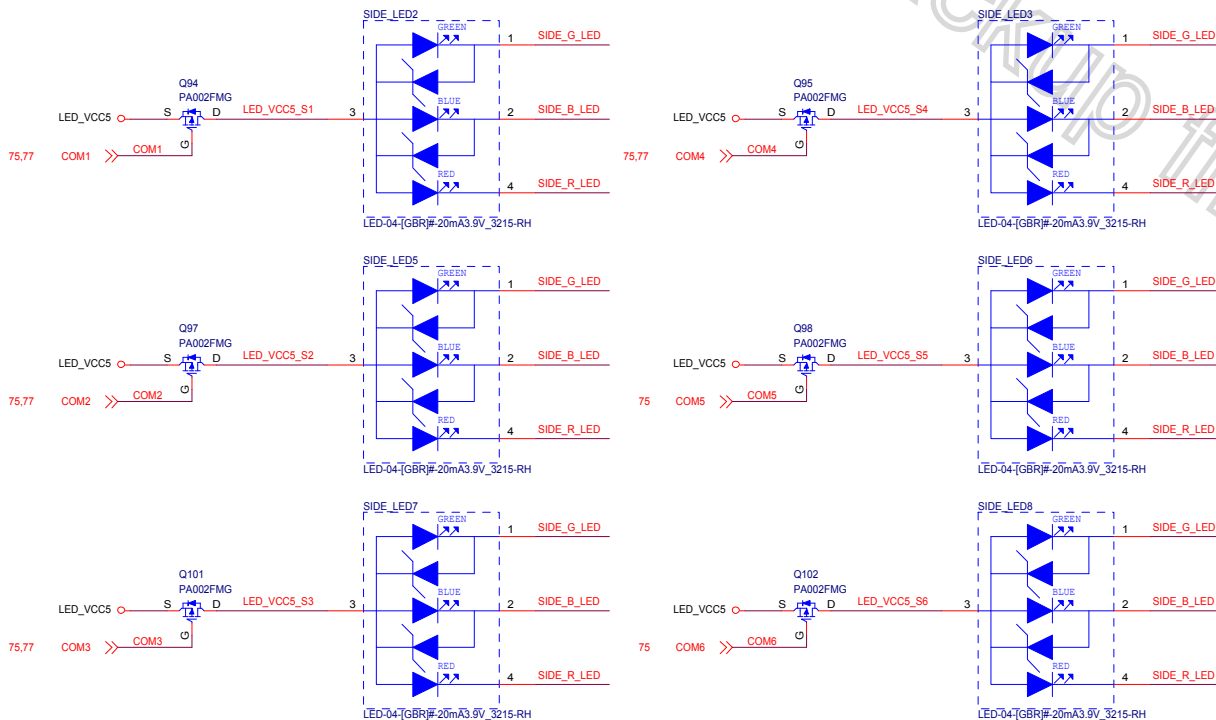
外接LED 燈條 (RGB )

--- PCB 文字面 (JLED1)

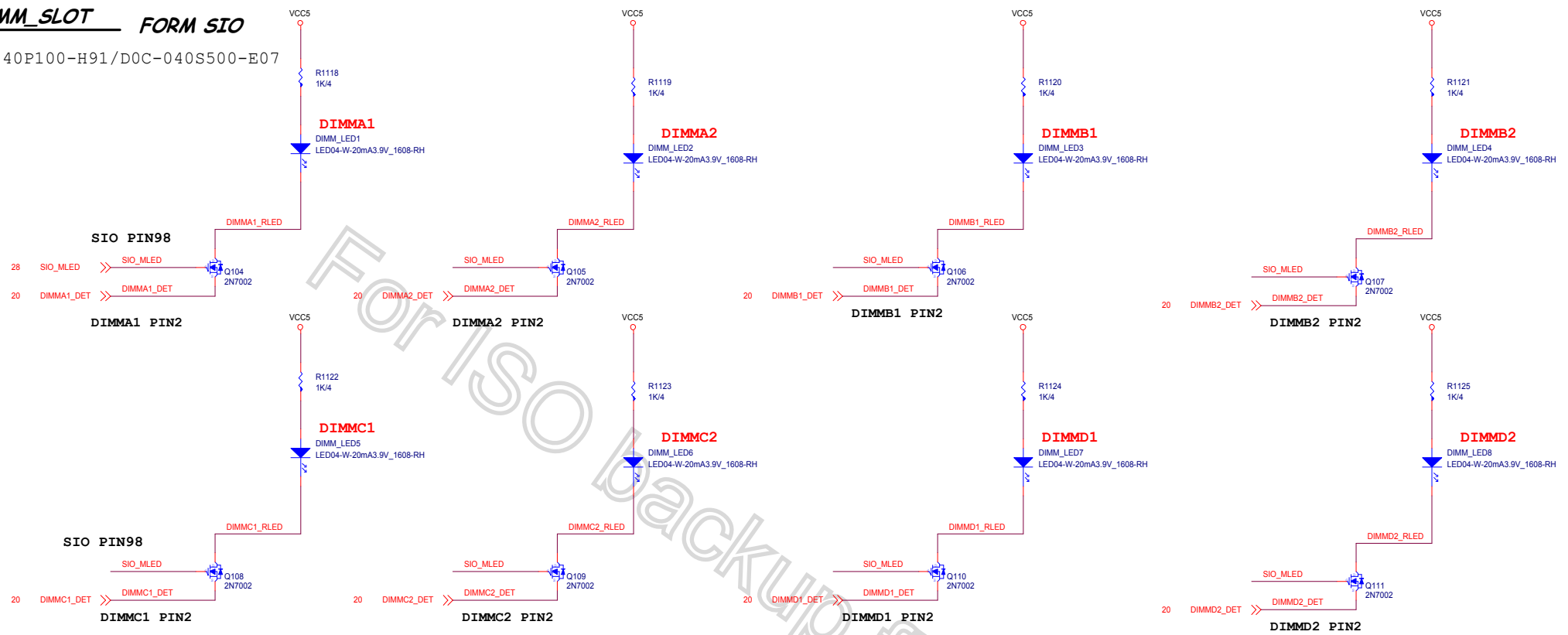
--- 手冊註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺 (待7A20驗證)

## BOARD SIDE LED \*8

DOC-040R700-H91  
Forward Current 20mA  
Pulse Forward Current 30-60mA

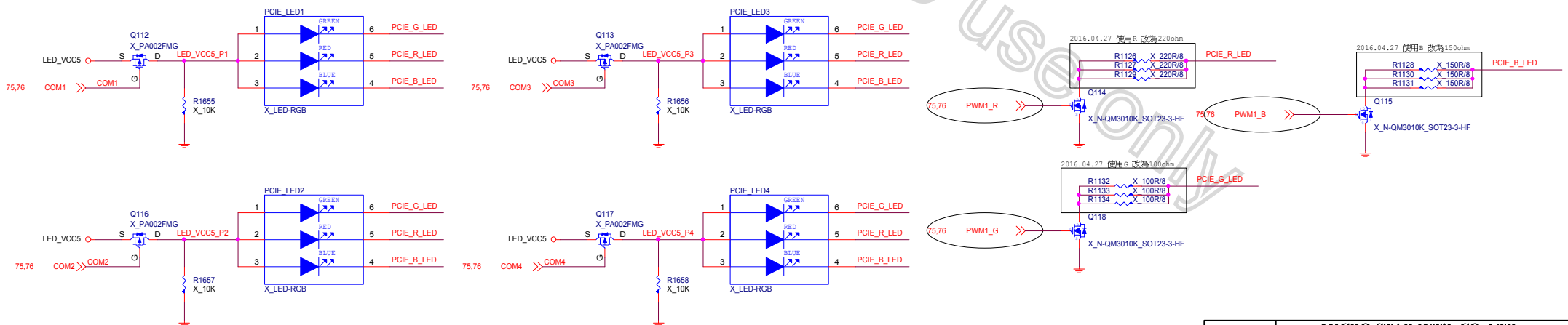


D0C-040P100-H91/D0C-040S500-E07



PCIE\_SLOT LED\*4  
FORM MCU

D0C-040S400-H91

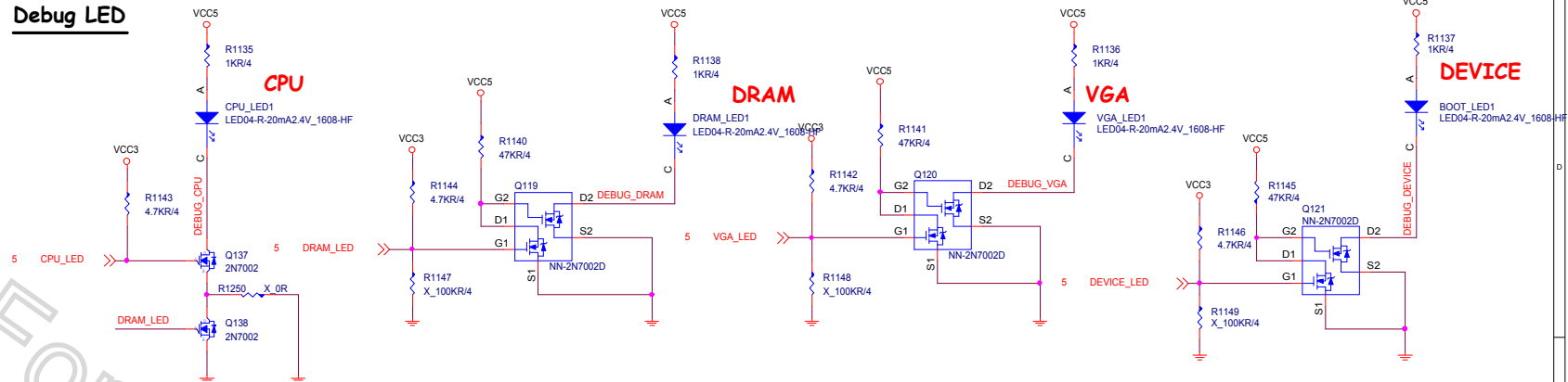


**MICRO-STAR INT'L CO.,LTD**

**MS-7B09**

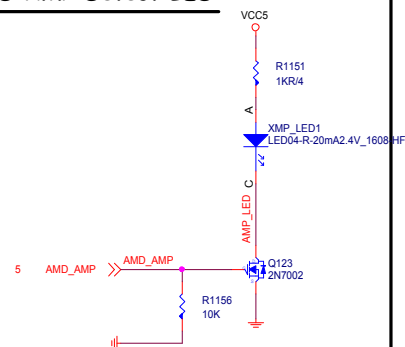
Size Custom	Document Description <b>LED DIMM/PCIE</b>	Rev 2.0
Date: Thursday, August 10, 2017		Sheet 77 of 87

## Debug LED

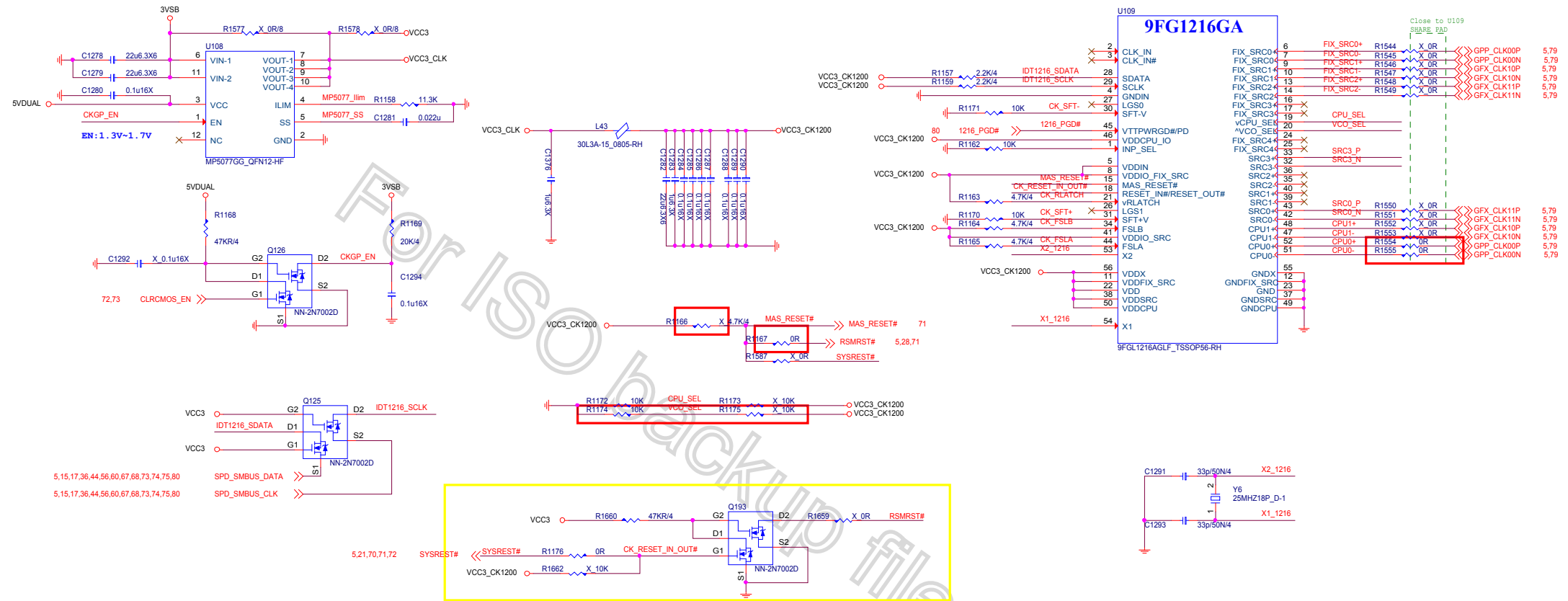


LED	GPIO	AGPIO84_0	AGPIO85_0	EGPIO84_1	EGPIO85_1
亮		GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅		GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

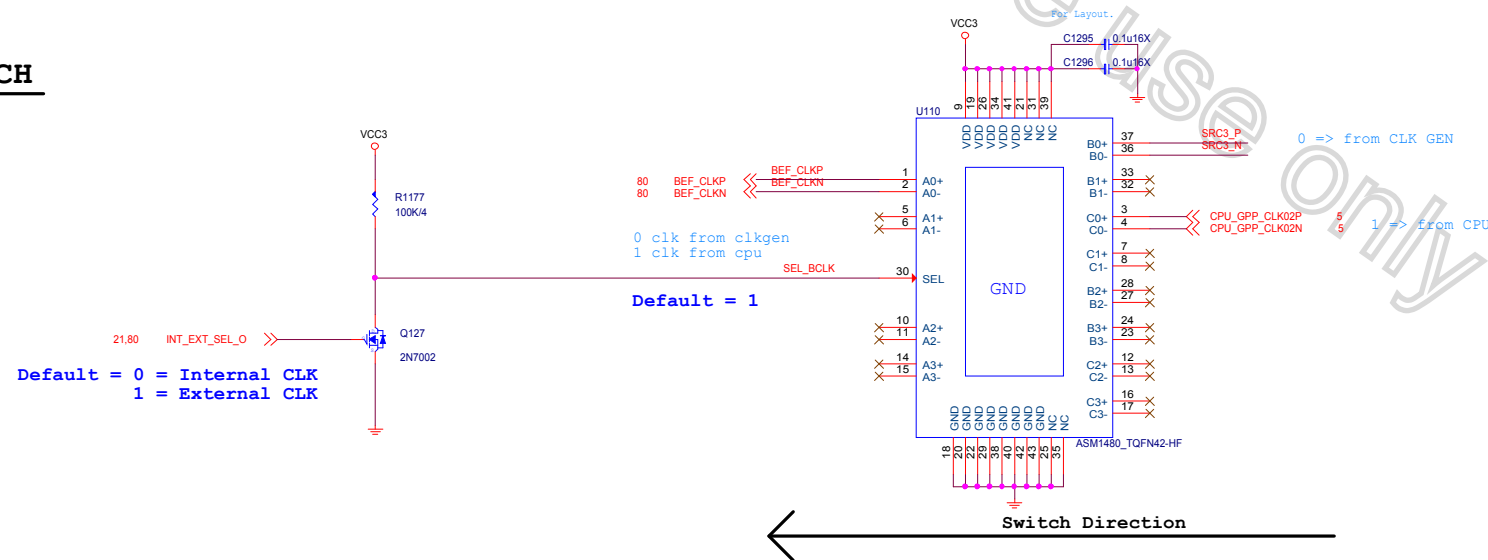
## AMD AMP Detect LED



## CLOCK GEN



## CLOCK SWITCH

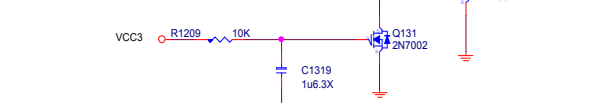
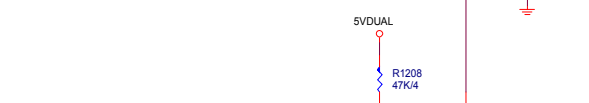
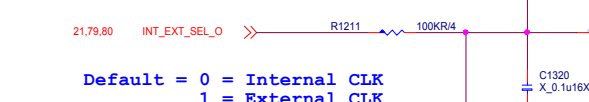
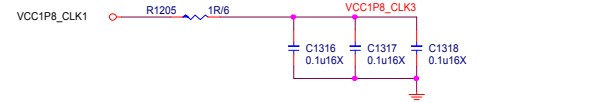
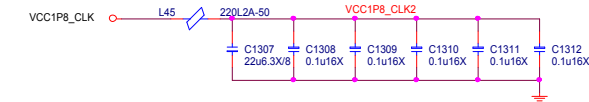
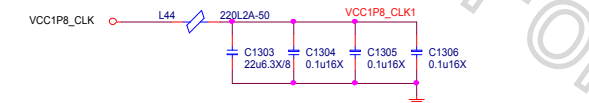
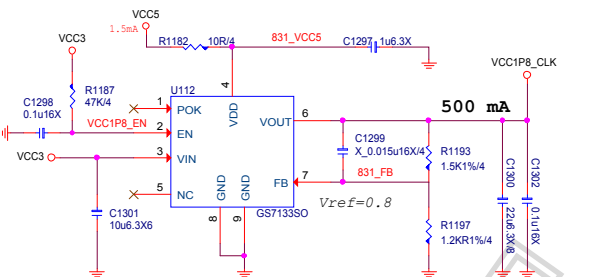


# CLOCK BUFFER

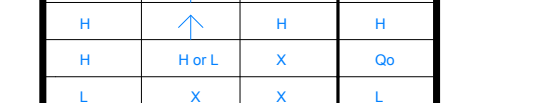
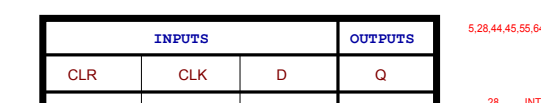
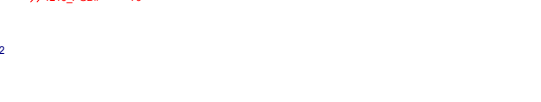
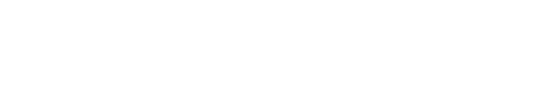
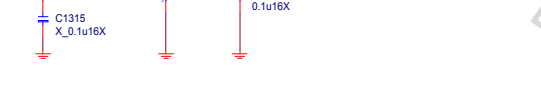
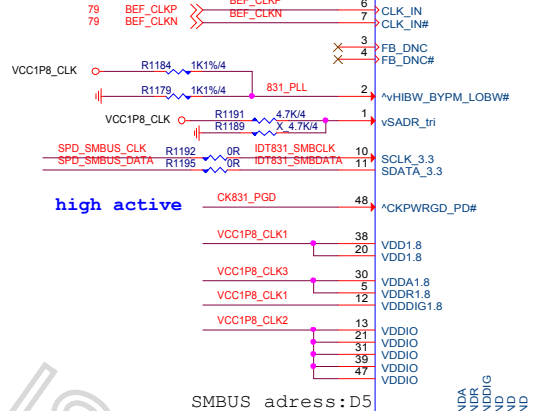
5,15,17,36,44,56,60,67,68,73,74,75,79  
5,15,17,36,44,56,60,67,68,73,74,75,79

SPD\_SMBUS\_CLK  
SPD\_SMBUS\_DATA

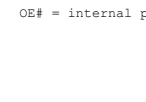
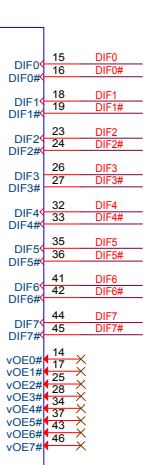
SPD\_SMBUS\_CLK  
SPD\_SMBUS\_DATA



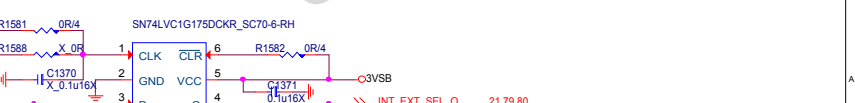
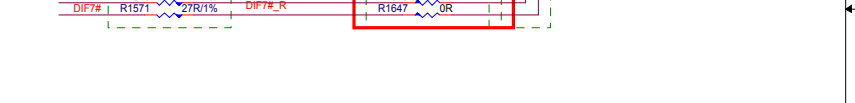
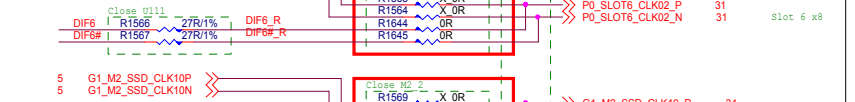
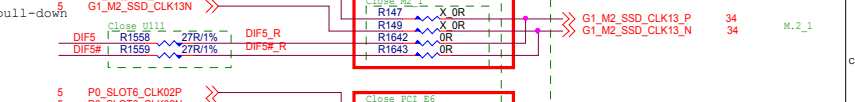
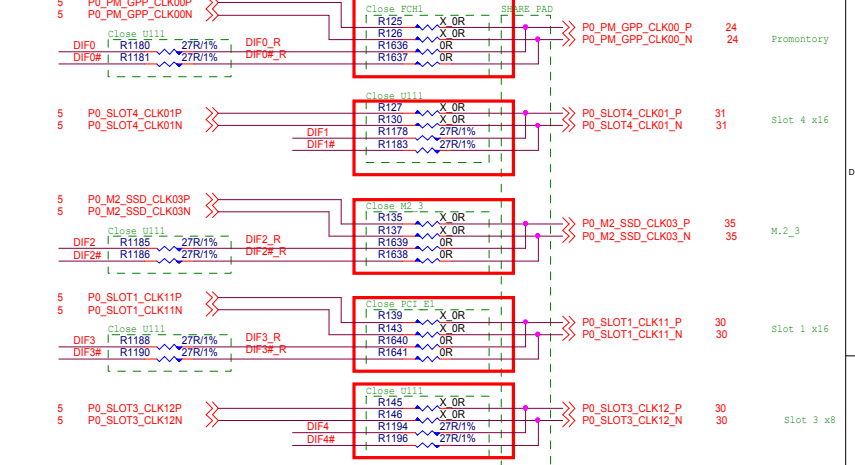
5,15,17,36,44,56,60,67,68,73,74,75,79



5,15,17,36,44,56,60,67,68,73,74,75,79

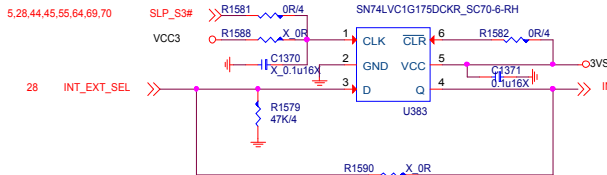


5,15,17,36,44,56,60,67,68,73,74,75,79

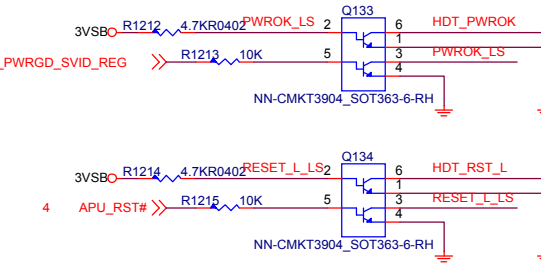
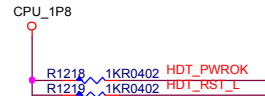
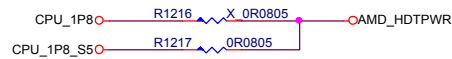


5,15,17,36,44,56,60,67,68,73,74,75,79

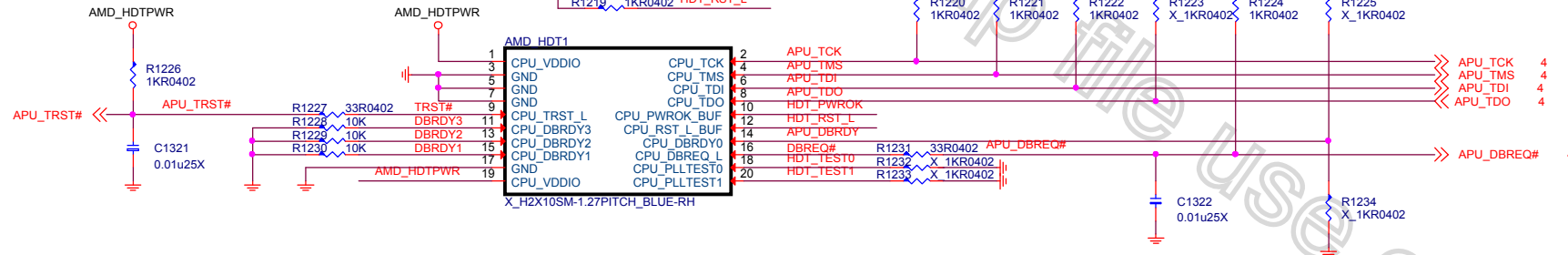
INPUTS			OUTPUTS
CLR	CLK	D	Q
H	↑	L	L
H	↑	H	H
H	H or L	X	Qo
L	X	X	L



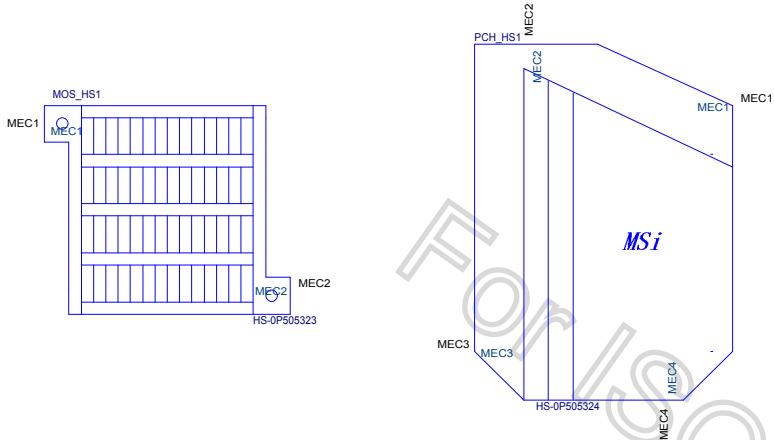
Stuff for first model



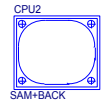
$$\begin{aligned} IB &= (AMD\_HDTPWR - V_{be}) / 4.7k \\ (1.8 - 0.95) / 4.7k &= 0.181mA \\ IC &= (V_c - V_{ce}) / 10k \\ (1.8 - 0.2) / 10k &= 0.16mA \\ IB &= (V_b - V_{be}) / 10k \\ (1.75 - 0.95) / 10k &= 0.08mA \\ IC &= (V_c - V_{ce}) / 10k \\ (3.3 - 0.2) / 10k &= 0.16mA \end{aligned}$$
$$\begin{aligned} B * Ib > Ic &= 10 * 0.181 = 1.81 > 0.16 \\ B * Ib > Ic &= 10 * 0.08 = 0.8 > 0.16 \end{aligned}$$



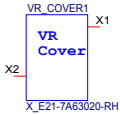
HEAT SINK



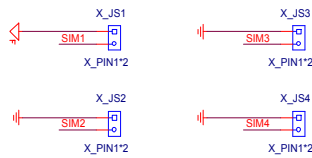
CPU Socket



VR COVER



Simulation



MANUAL PART

AMI1  
AMI LABEL  
G51-M1SPXXA-A09

MKT1  
Label  
G51-M1SPM07-Q13

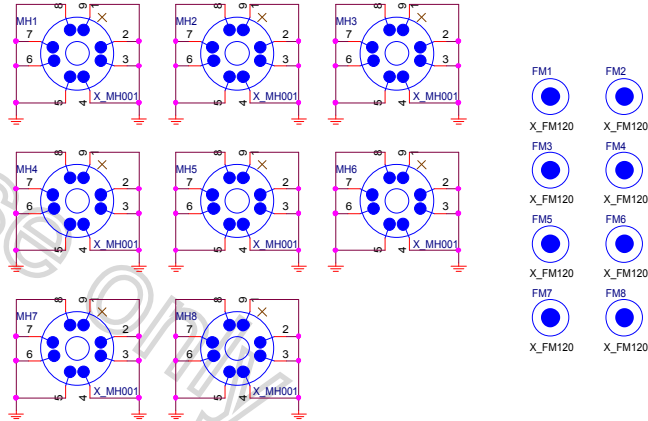
SLI1  
Label  
Y01-RNVIDIN-000

BAT1\_X1  
BAT-QR2032  
D06-0105101-K26



VER: 2.0 --> 601-7B09-03S

Optics Orientation Holes



Add for EMI

